MONOLITHIC SHORT WAVE INFRARED (SWIR) DETECTOR ARRAY

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16. Abstract

A monolithic self-scanned linear detector array is being developed for remote sensing in the 1.1- to 2.4-μm spectral region. A high-density IRCCD test chip has been designed and fabricated to verify new design approaches required for the detector array. The driving factors in the Schottky barrier IRCCD (Pd_2Si) process development are the attainment of detector yield, uniformity, adequate quantum efficiency, and lowest possible dark current consistent with radiometric accuracy. A dual-band (512 detectors per band) module has been designed that will consist of two linear detector arrays. The sensor architecture (called center tap architecture) places the floating diffusion output structure in the middle of the chip, away from the butt edges. A focal plane package has been conceptualized that includes a polycrystalline silicon substrate carrying a two-layer, thick-film interconnecting conductor pattern and five epoxy-mounted modules. A polycrystalline silicon cover encloses the modules and bond wires, and also serves as a radiation and EMI shield, thermal conductor, and contamination seal. Bench test and calibration equipment have been assembled to test and evaluate the electronics, optics, and scene simulator. A correlated double sampler reduces noise.

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Section 1

INTRODUCTION

1.1 STATEMENT OF WORK

The information presented in this report is a summary of the Design Trade Study for the Short Wave Infrared Monolithic Array Development program (NASA contract NAS5-27800). The objective of this 24-month program is the development of a monolithic self-scanned linear detector array technology for remote sensing in the 1.1- to 2.4-μm spectral region. The basic linear imager will be a monolithic, integrated circuit chip with two detector arrays, associated multiplexers, and output buffer amplifiers. These modules will be buttable so that they may be assembled together to form linear arrays of several thousand detectors. Each array will be optimized to operate in a different band in the short wave infrared (SWIR) spectral region. RCA is developing the Pd_2Si Schottky barrier IRCCD technology for this application.

A proof-of-concept pushbroom focal plane will be developed and evaluated. The Test Assembly will consist of five butted modules and associated control electronics. This deliverable imager will have two linear detector arrays with 2,560 detectors each. The detector cross-track center-to-center spacing will be 30 μm. The signal-to-noise requirement of the Test Assembly is 110 at the specified SWIR wavelengths and working level irradiance (WLI). The nominal operating temperature of the Pd_2Si Schottky barrier IRCCD technology for this radiometric application is 120K. The power dissipation budget at 120K is 27 μW per detector.

1.2 REPORT OVERVIEW

The Design Trade Study Report is divided into five technical sections. The sections are entitled:

- Section II – High-Density Test Chip Evaluation
- Section III – Schottky Barrier IRCCD (Pd_2Si) Process Development
- Section IV – Dual-Band Module Design
- Section V – Test Assembly Design
- Section VI – Bench Test and Calibration Equipment.

Section II describes the measurements performed on the high-density IRCCD test chip. This integrated circuit was designed and fabricated to verify new design approaches required for the dual-band module. The test chip utilizes 30-μm center-to-center detector and CCD cross-track pitch; low-power, low-noise amplifier designs; and new input/output CCD layout techniques.

Section III details the Pd_2Si IRCCD process development. A driver in the process optimization has been the attainment of detector yield and uniformity equivalent to that attained in the more mature PtSi Schottky barrier process. A second driver has been achieving adequate quantum efficiency at 2.22 μm (the long wavelength band of interest) to meet the signal-to-noise requirement.

Section IV presents the dual-band module architecture and highlights the design features. The tradeoffs leading to the final design approach are discussed. The projected sensor performance is presented.

Section V discusses the Test Assembly design. The development of the hybrid substrate thick-film technology is presented in detail. The substrate dimensions, the issues concerning filter placement, and the interface considerations are discussed. Also, the module alignment procedure is presented.

Section VI provides an overview of the Bench Test and Calibration Equipment (BTCE). The BTCE section describes the module drive electronics, the optical test configuration, and the scene simulator. The initial test results of the low-noise signal conditioning Correlated Double Sampler (CDS) are discussed.

Section 2

HIGH-DENSITY TEST CHIP EVALUATION

2.1 INTRODUCTION

A high-density Schottky barrier IRCCD linear array was designed and fabricated by RCA in 1982. This 250-x-125-mil test chip has provided and will continue to provide very useful data on performance of high-density designs. The test chip (designated TA11395) is a shortened version of the baseline design for the NASA Short Wave Infrared (SWIR) Detector Array.

The TA11395 is a 192-detector linear array with a 30-μm center-to-center detector pitch. The test chip is shown in Fig. 2-1. The detector readout consists of a parallel-to-serial buried-channel, double polysilicon CCD shift register. Adjacent to the Schottky output register is a companion CCD register with a fill-and-spill input layout orthogonal to the register as required for end-to-end abutment of imagers. A schematic of the chip is given in Fig. 2-2.

The test chip has three floating diffusion outputs. Two of the outputs employ a new, low-power NMOS amplifier design. These amplifiers are the output circuitry for the detector register and the companion register. The third output is a buried-channel NMOS amplifier design. This output circuit will be used to investigate a combined single-stage, on-chip amplifier/JFET buffer for low noise performance.

As of this writing the following has been demonstrated. First, the 192-stage output register has been operated with electrical word input at room temperature. A single output pulse may be seen in Fig. 2-3. The register exhibits adequate dynamic range and good transfer efficiency for the anticipated SWIR application ($Q_{MAX} \approx 1 \times 10^6$ electrons). Second, the low-power amplifiers exhibit adequate slew rate for typical earth resources applications. Third, the low-power amplifiers operate with excellent on-chip power dissipation of approximately 4.5 mW.

The following sections detail the measurements that have been made to date on the test chip. It is planned that additional measurements will be made during the second quarter of 1983 to assess the test chip's imaging capability.

2.2 CCD REGISTER PERFORMANCE

Close examination of the TA11395 CCD characteristics provided information on optimum operating conditions and provided detailed performance data. A square wave electrical input word applied to the test chip CCD register input results in the signal output as shown in Fig. 2-4. By varying the amplitude and level adjustments of the CCD clock phases, the input source, and the dc gate structures, proper operation and maximum signal output may be ensured.

The directionality of charge transfer is assured by proper adjustment of the gate and register voltages. As a check on the conditions considered to give best operation, these voltages were converted to V_{MB} potentials (V_{MB} is the CCD channel potential with respect to substrate, the V_{MB} level varies with applied gate potential). The transfer functions were measured to be:

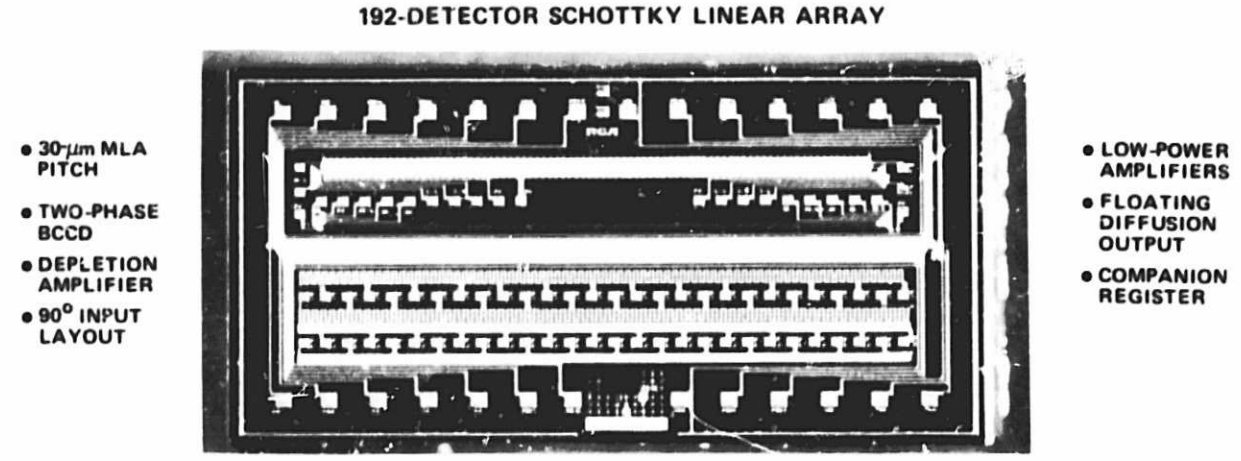


Fig. 2-1. The TA11395 chip.

$$V_{MBP1} = 0.9\, V_{P1} + 8$$

and

$$V_{MP2} = 0.9\, V_{P2} + 9.4$$

where $V_{MBP1} = V_{MB}$ for a poly 1 gate

$V_{MBP2} = V_{MB}$ for a poly 2 gate

V_{P1} = poly 1 gate voltage

V_{P2} = poly 2 gate voltage

These transfer functions were obtained by measurements of V_{MB} potentials on the TA11395 CCD register. The CCD was made conductive first by varying poly 1 gates while holding poly 2s at 10 V and then varying poly 2 gates while holding poly 1s at 10 V.

A table of the V_{MB} potentials demonstrated to give best CCD performance is given in Table 2-1. A plot of the V_{MB} gate potential levels, along with the input source and output drain potentials is given in Fig. 2-5. From the plot it may be seen that the input fill-and-spill operating potentials and the floating diffusion reset potentials are indeed compatible with the CCD register operating conditions. The nominal potential step in the channel is shown to be 4 V.

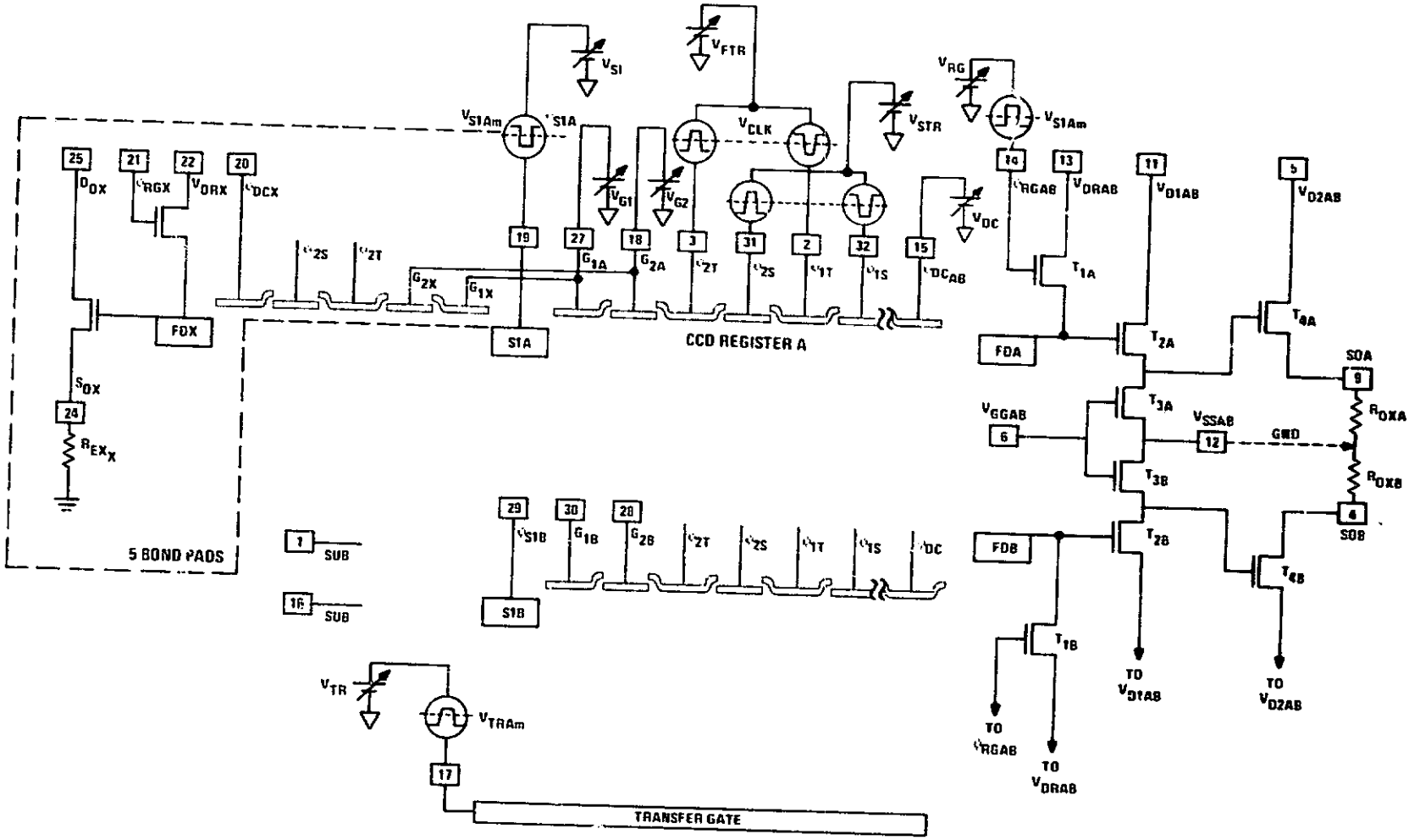


Fig. 2-2. Schematic of TA11395.

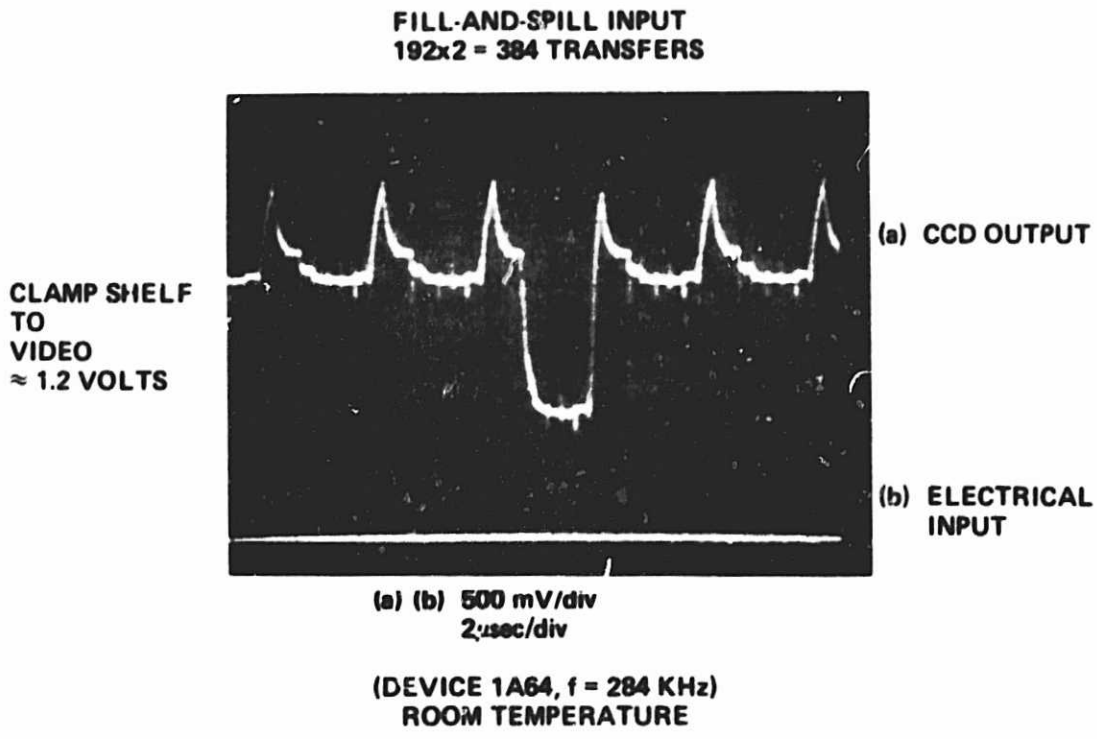


Fig. 2-3. An example of output pulse resulting from electrical word input at room temperature.

With proper device functioning assured, the CCD transfer efficiency was determined. In CCD devices the transfer inefficiency, ϵ, is commonly measured rather than the efficiency. When using a square wave electrical input signal, ϵ is most evident immediately following a transition in the input signal level. If the transition from low to high level is utilized, the inefficiency may be computed by the ratio of ΔV to V, with these quantities depicted in Fig. 2-6.

The value of ϵ is calculated employing the relationship, $n\epsilon = \Delta V/V$ where n = number of transfers (n = 192x2 for TA11395). For the test device, ΔV was found to be 5 mV out of a total V = 520 mV. The transfer inefficiency was thus found to be $\epsilon = 3 \times 10^{-5}$. This value of ϵ was for room temperature operation and is expected to increase only slightly at 120°K operation.

The floating diffusion capacitance, C_{FD} at room temperature, was determined by measuring the rms signal current, I_S (nanoamperes), at the CCD drain output due to the rms charge being transferred to the C_{FD}. A sensitive electrometer connected in series with a shielded 18-V drain supply was used (see Fig. 2-7). The C_{FD} was calculated using the expression

$$C_{FD} = \frac{I_S t}{\Delta V_{FD}}$$

where t = the time required for one charge transfer

ΔV_{FD} = the output voltage divided by the gain of the on-chip amplifier.

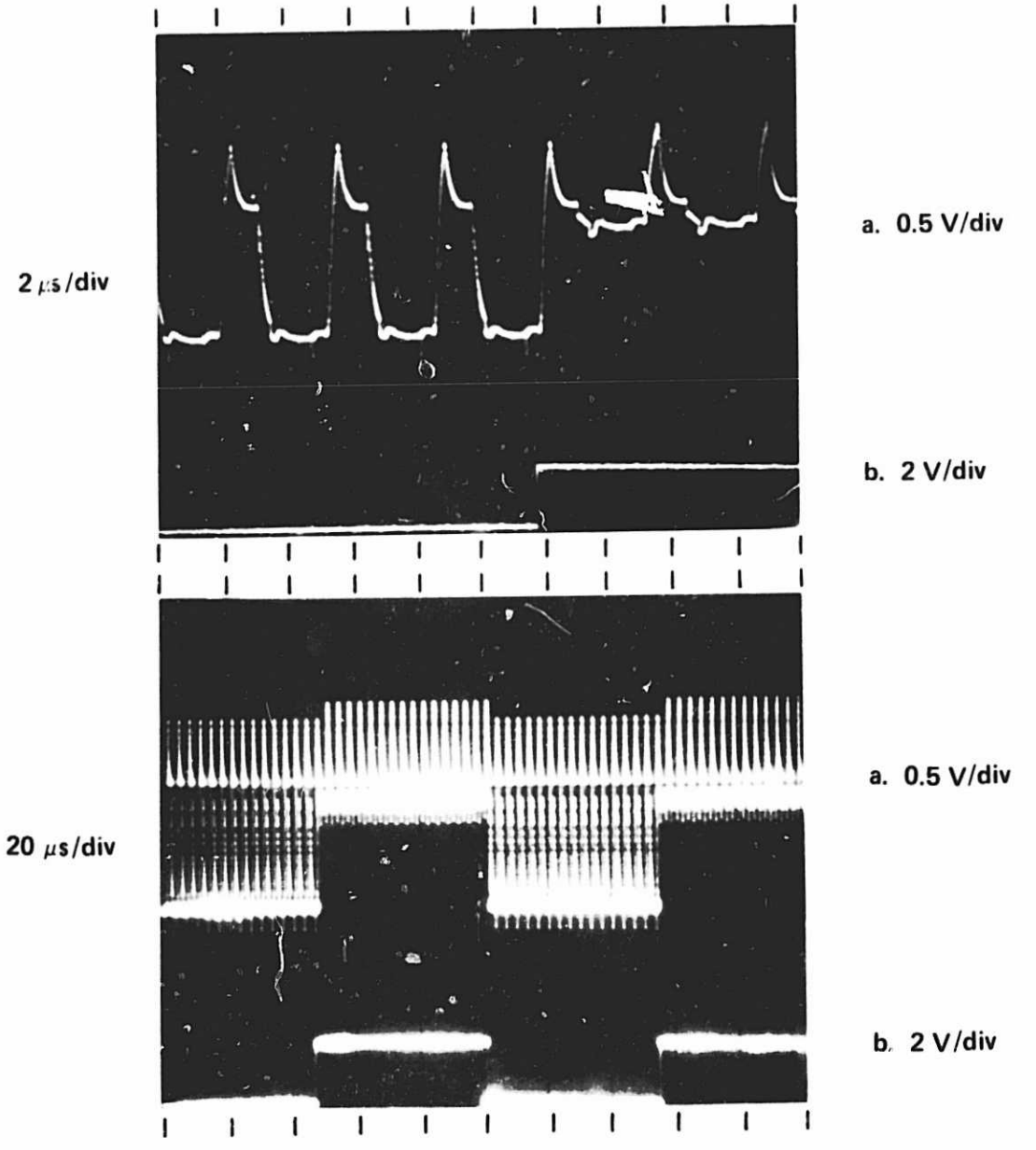


Fig. 2-4. Operational CCD register response to applied square wave.

TABLE 2-1. OPERATIONAL V_{MB} FOR CCD TA11395

	V Gate High	V_{MB} High	V Gate Low	V_{MB} Low
Source	10.8	10.8	3.5	3.5
G1 Poly 2 Gate Input	-2.0	7.6	-4.2	5.6
G2 Poly 1 Gate Input	1.5	9.4	1.5	9.4
ϕ_{2T} Poly 2 Gate/Register	2.4	11.6	-12.0	-1.4
ϕ_{2S} Poly 1 Gate/Register	9.0	16.1	-5.2	3.3
ϕ_{1T} Poly 2 Gate/Register	2.4	11.6	-11.8	-1.2
ϕ_{1S} Poly 1 Gate/Register	9.0	16.1	-5.0	3.5
ϕ_{DC} Poly 2 Gate Output	-4.5	5.6	-4.5	5.6
ϕ_{RG} Poly 1 Gate Output	5.0	12.5	-2.0	6.2
V_{DR} Drain	12.4	12.4	12.4	12.4

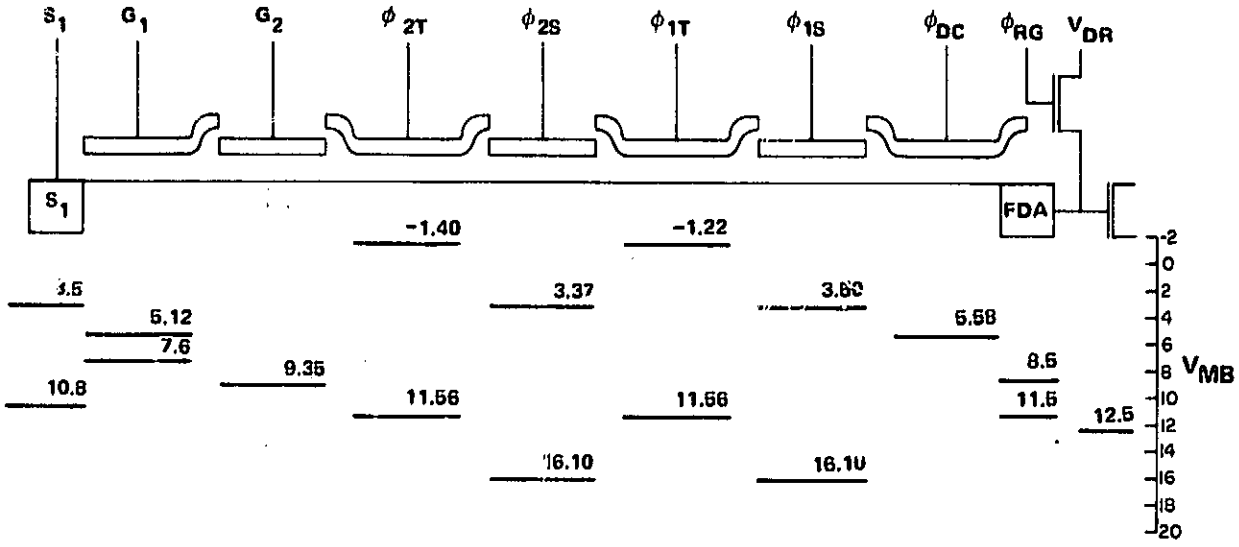


Fig. 2-5. Operational device V_{MB} levels for TA11395.

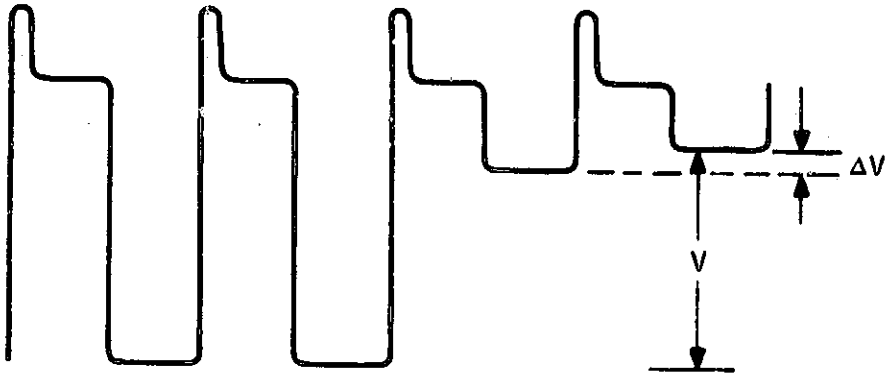


Fig. 2-6. Efficiency measurements.

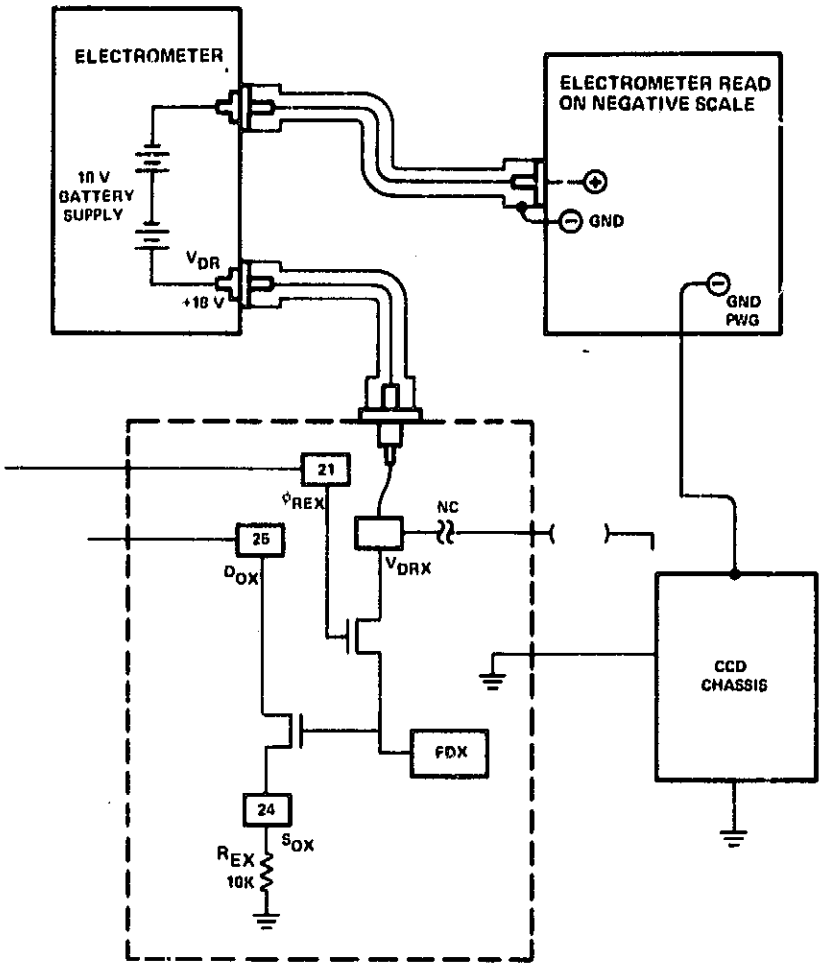


Fig. 2-7. Setup to measure signal charge from buried-channel stage.

For the TA11395 device operating at a 284-kHz clock rate $t = 3.5 \times 10^{-6}$ s. Taking a ΔV_{FD} at half full-well capacity, $\Delta V_{FD} = 0.95$ and $I_S = 17.5$ nA, the resulting floating diffusion capacitance is $C_{FD} = 0.065$ pF. This value agrees closely with predictions based on the layout of the floating diffusion output. With the value of the floating diffusion capacitance known, the charge capacity of the register was computed. The full-well charge capacity was shown to be:

$$N_e = \frac{C_{FD}\ V_{FD}^{max}}{q}$$

or

$$N_e = \frac{0.065 \text{ pF} \times 1.9 \text{ V}}{1.6 \times 10^{-19} \text{ c/e}}$$

$$N_e = 770{,}000 \text{ electrons}$$

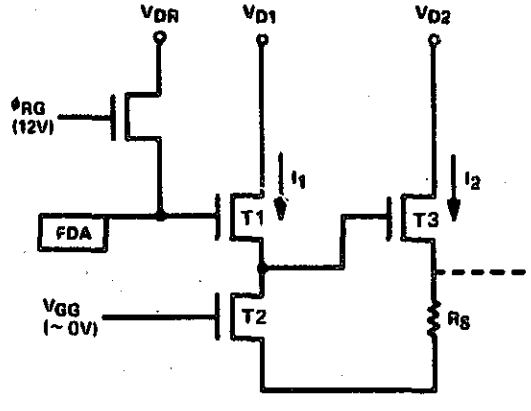
The storage gate dimensions of the TA11395 CCD register are 10-x-32 μm. Thus, the charge capacity of the buried n-channel register is 2.4×10^{11} electrons/cm^2.

2.3 ON-CHIP ENHANCEMENT AMPLIFIER

The surface channel enhancement FET amplifier is a two-stage source follower design (shown in Fig. 2-8), having a final stage external load resistor which is placed off the focal plane to reduce power dissipation. The amplifier was designed during the MLA Instrument Definition Study employing R-CAP (RCA circuit analysis program).

The amplifier was characterized by measuring its linearity, gain, power dissipation, slew rate, and output noise. The amplifier for the main CCD register of devices, TA11395-1A64 and TA11395-1B40, were the particular circuits analyzed. The characteristics of both devices were essentially identical. The linearity of the amplifier is displayed in the V_{out} versus V_{in} curves on Fig. 2-9. Three values of load resistance, R_S, were used: 3.9K, 6.0K, and 10.0K ohms. The gain and range over which ≤1% nonlinearity exists, for each resistance value, are also indicated. The 10K-ohm R_S provides the largest gain and a linear range of 2.3 V. Using this value of R_S the first and second drain voltages – V_{D1} and V_{D2} – were varied to determine optimum operating voltages. The optimum is that set of voltages yielding the greatest linearity, where any further increase in voltage produces only a marginal increase in linearity. This criterion simultaneously minimizes power dissipation. As indicated by Fig. 2-10, the intermediate voltage settings were chosen as optimum for this design. The gain was measured to be 0.553.

Power dissipation for the amplifier was measured with R_S = 10K ohms and three sample settings of V_{D1} and V_{D2}. As indicated by the P_{TOTAL} column of Fig. 2-11, the dissipation is lower than the RFP goal of 11.9 mW. The nominal voltage settings, chosen on the basis of linearity and power, are V_{D1} = 15 and V_{D2} = 12. The on-chip amplifier power dissipation for the nominal conditions is only 4.5 mW.



DEVICE	W (μm)	L (μm)
T1	6	14
T2	6	14
T3	38	13

Fig. 2-8. SCCD design.

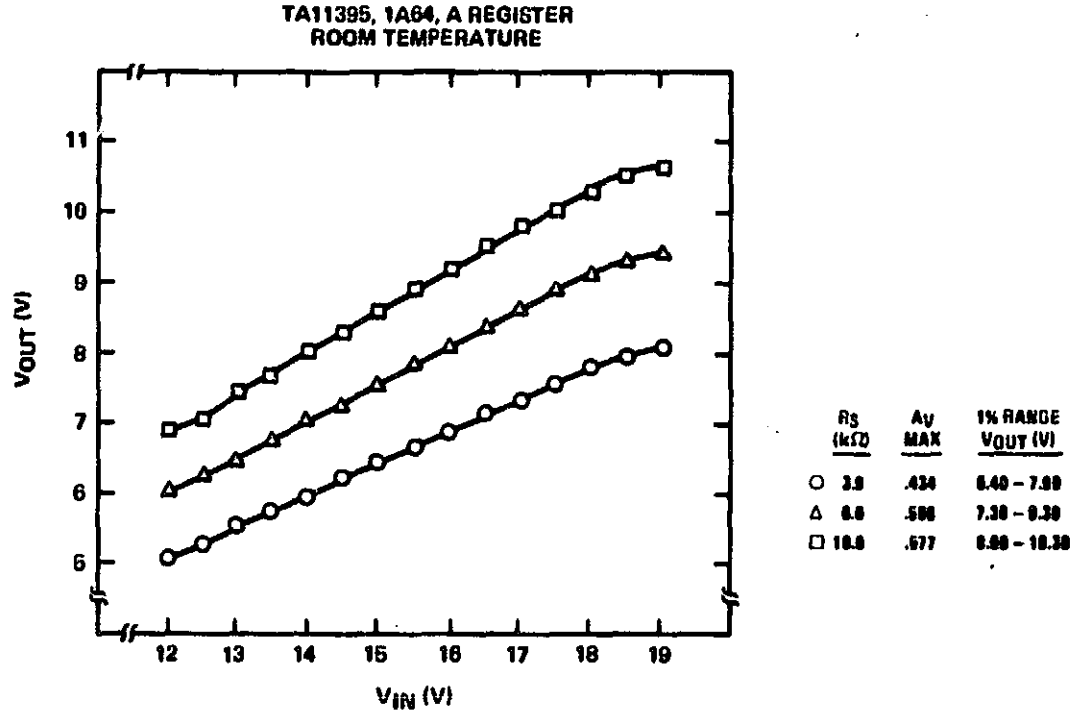


Fig. 2-9. Enhancement amplifier linearity for different load resistors.

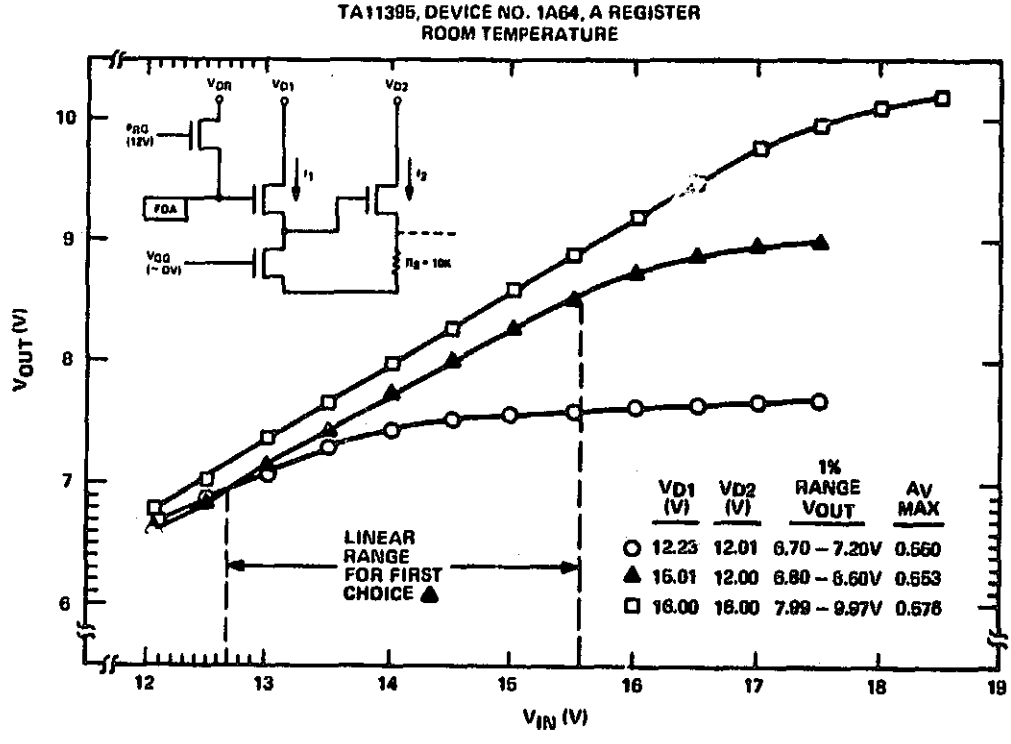
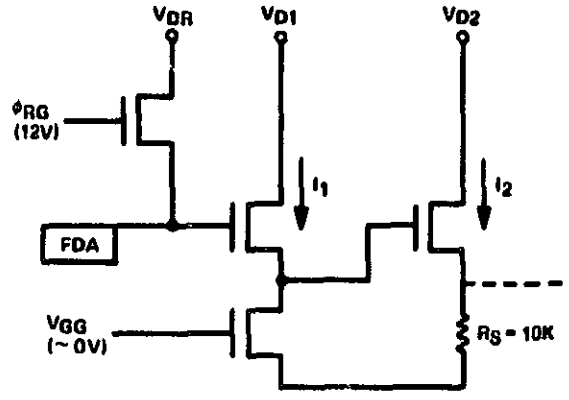


Fig. 2-10. Enhancement amplifier gain vs. drain supply voltages.



	V_{D1} (V)	V_{D2} (V)	I_1 (μA)	I_2 (μA)	P_1 (mW)	P_2 (mW)	P_{TOTAL} (mW)
(a)	17.037	15.150	150	630	2.56	5.58	8.14
(b)	12.108	11.900	150	597	1.82	3.54	5.36
(c)	15.05	12.00	67	705	1.00	3.50	4.50

ROOM TEMPERATURE
(a & b), V_{DR} · 19.7V
(c), V_{DR} = 14.5V

RFP AMPLIFIER DISSIPATION GOAL = 11.9 mW
(27.4 mW/MODULE)

Fig. 2-11. Enhancement amplifier on-chip power dissipation.

The slew rate of the amplifier can be seen by the rise and fall time displayed by the video CCD output signal (see Fig. 2-12). It is estimated that the slew rate is on the order of 5 V/μs. The output noise characteristics of the amplifier were measured and compared to the output noise of a buried-channel FET amplifier. These measurements are discussed in Section 2.4.

Table 2-2 summarizes the measured enhancement amplifier characteristics just discussed.

TABLE 2-2. DEVICE TA11395-1A64-A AMPLIFIER CHARACTERISTICS

Linear Range (≥99%)	2.3 V
Gain	0.553 V_{D1} = 15 V, V_{D2} = 12 V
Power Dissipation	4.5 mW
Slew Rate	5 V/μs

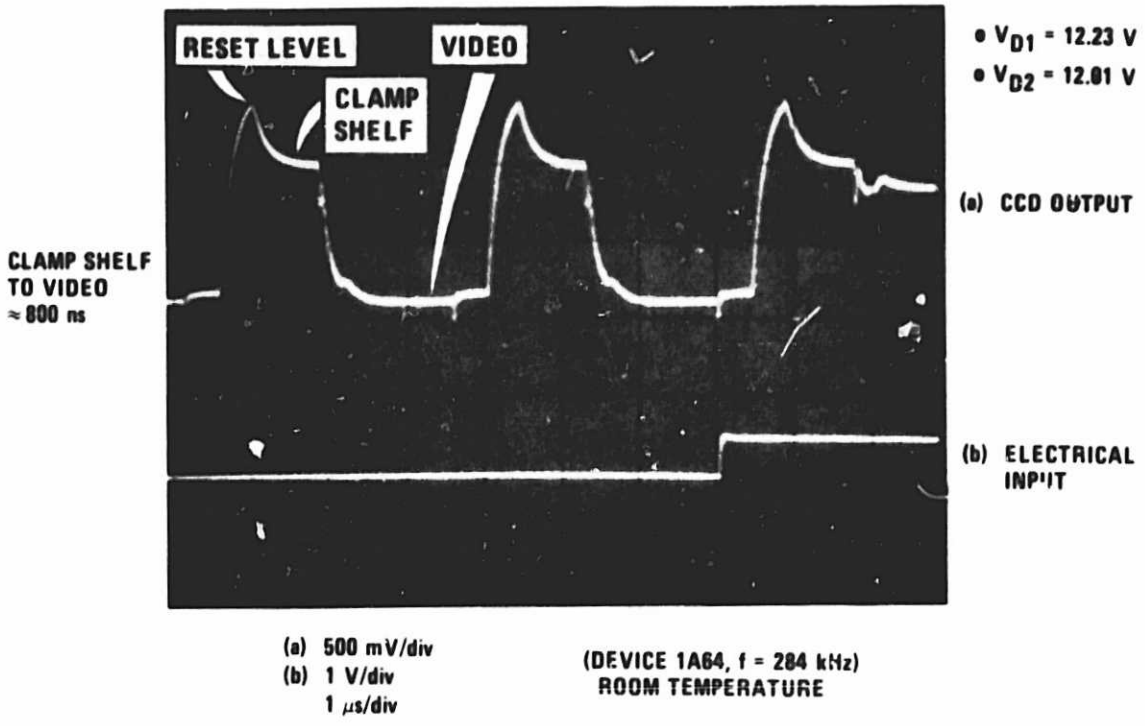
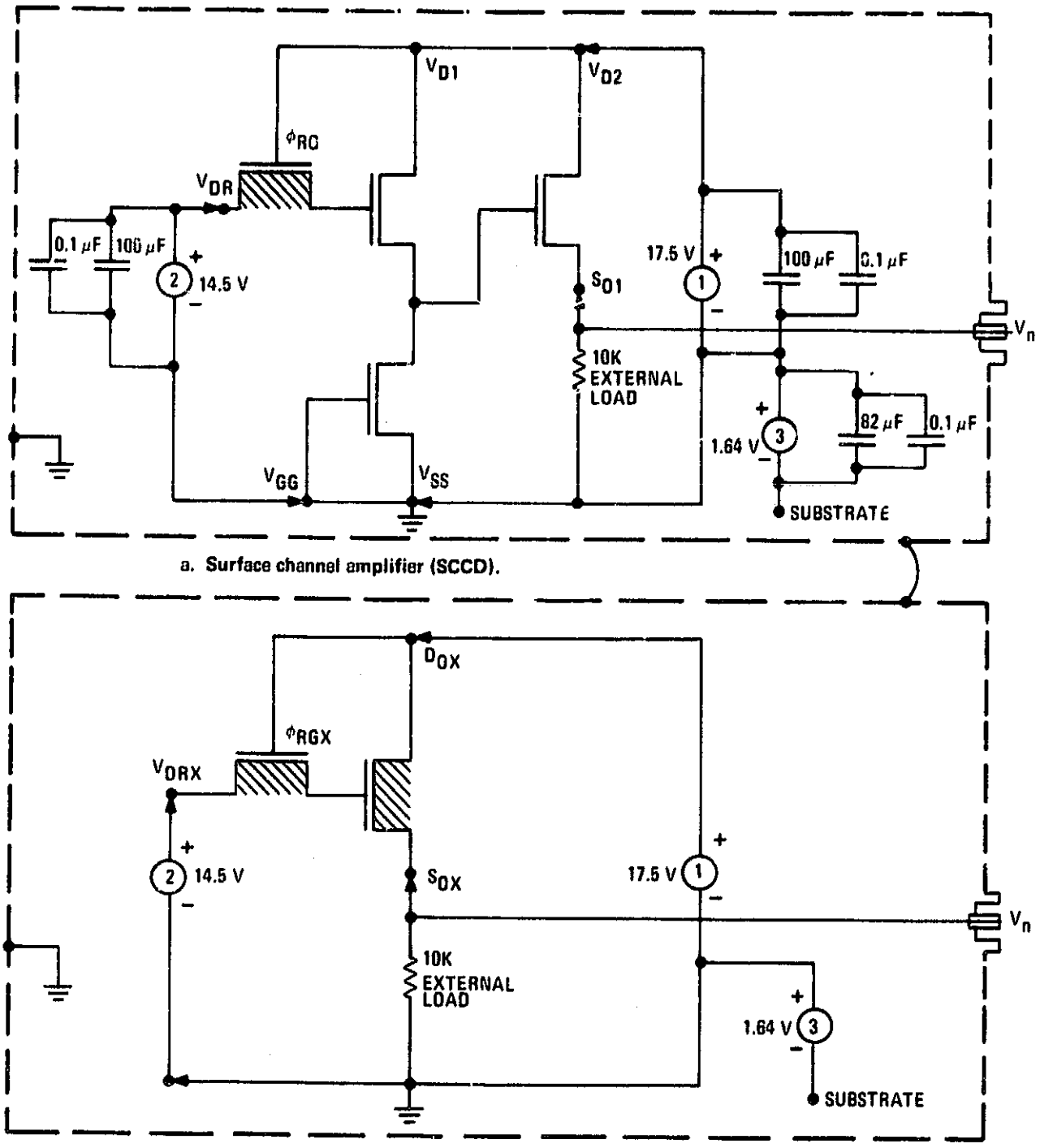


Fig. 2-12. TA11395 pixel output at low drain supply voltages.

2.4 BCCD FET AMPLIFIER

Amplifier output noise measurements were performed to evaluate the buried-channel FET (depletion device) single-stage source follower as an alternative to the surface-channel (enhancement) FET two-stage source follower. The depletion FET would be coupled in the test assembly with a low-noise JFET buffer amplifier to provide an output drive impedance comparable to that of the two-stage source follower. These measurements concluded that for a bias ≥12 V applied to the input gates of both amplifiers, the 1/f noise corner frequency of the depletion device is 90 kHz. No corner frequency is evidenced out to the measurement equipment limit of 220 kHz by the enhancement amplifier. These results are consistent with previous RCA measurements which indicated significantly lower noise for depletion FET devices (BCCD) than achieveable with enhancement FET devices (SCCD).

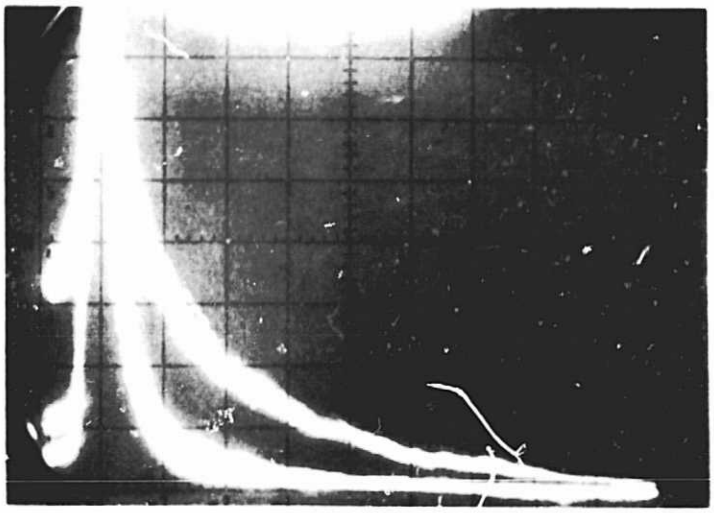
The schematics of the measurement setups used to evaluate the BCCD FET and SCCD two-stage amplifier are shown in Fig. 2-13. A chip (TA11395) with SCCD and BCCD on a common substrate was mounted in a Textool Socket, provided with battery supplies 1, 2, and 3 (for biasing), and enclosed in an aluminum box for electromagnetic shielding; thus, this eliminated power supply and external noise sources. Low- and high-frequency capacitive filters were provided to minimize drain noise crossover between amplifiers while both amplifiers were energized. Two TA11395 test devices from the same processing lot (1A64 and 1B40) were evaluated. The spectral noise at the output of the SCCD is shown in Fig. 2-14 as the upper traces on a spectrum analyzer (10-kHz resolution). The BCCD noise spectrum is displayed on the lower traces. To obtain better resolution the noise spectrum was measured using an amplifier (spectral gain characteristics previously measured), coupled to a wave analyzer. The noise data were taken for



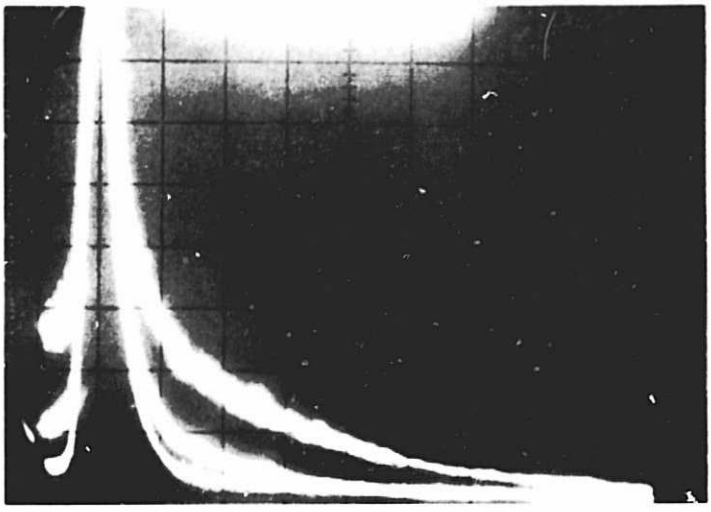
a. Surface channel amplifier (SCCD).

b. Buried-channel amplifier (BCCD).

Fig. 2-13. Schematics of measurement setups.



a. Device TA11395 1A64.



L. Device TA11395 1B40.

Fig. 2-14. Amplifier noise spectrum.

device TA11395-1A14 and is plotted in Fig. 2-15. A 200-Hz bandwidth was employed at each measurement frequency. In addition to the 90-kHz corner frequency described previously it is evident that the BCCD amplifier noise at the 1/f corner frequency is 16 $nV/\sqrt{Hz}$ which is 25 $nV/\sqrt{Hz}$ less than the SCCD. The corner frequency is in agreement with that measured by Brodersen and Emmons.[1] For comparison, measurements were made on a BCCD with lower depletion implant level. The data for this BCCD is also plotted in Fig. 2-12.

Time domain measurements of the noise were made as another means of investigating the relative noise characteristics. The wideband (1-MHz) noise shown in Fig. 2-16a is that of the SCCD, and in Fig. 2-16b that of the BCCD. Figure 2-17 shows the reduction in low-frequency noise and peak-to-peak noise amplitude resulting when the noise is passed through a 1-kHz low-pass filter. This indicates the reduced noise amplitude that would result when operating in cascade with a correlated double sampler with a 1-kHz low-pass characteristic.

Further output noise measurements indicate that the BCCD amplifier noise level increases with increasing input impedance and decreases with decreasing gate potential. The schematic of the measurement setup used is essentially the same as that shown in Fig. 2-11b, except that power supply 2 is replaced with a variable supply (without capacitive filters) and a resistor connected from the positive terminal to V_{DRX}. Using two values for Z_{IN} — 10K and 61.1K ohms — the peak-to-peak noise voltage, V_n at selected values of V_{DRX} is plotted in Fig. 2-18. It is seen that at V_{DRX} = 14.5 V, Z_{IN} = 61.1K, the measured noise output is then 0.32 mV peak-to-peak. This is 0.09 mV larger than the expected noise if one assumes that the only increase in noise will be due to resistor Johnson noise. The total noise due to both noise sources may be calculated employing the equation:

$$V_{ne}^2 = V_R^2 + V_{BCCD}^2$$

where V_R = P-P thermal noise contributed by input resistor

V_{BCCD} = P-P BCCD noise without input resistor.

The peak-to-peak thermal noise contributed by the input resistor, V_R, is 0.16 mV calculated using the expression

$$V_R = 10\sqrt{KTBR}$$

where K = Boltzmann's constant, 1.38×10^{-23} Joules/°K

T = 300°K

B = Bandwidth (1 MHz)

R = Resistance in ohms (61.1K)

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1. R. Brodersen and S. Emmons, "Noise in Buried-Channel Charge-Coupled Devices," IEEE Transactions on Electron Devices, vol. ED-23, no. 2, February 1976.

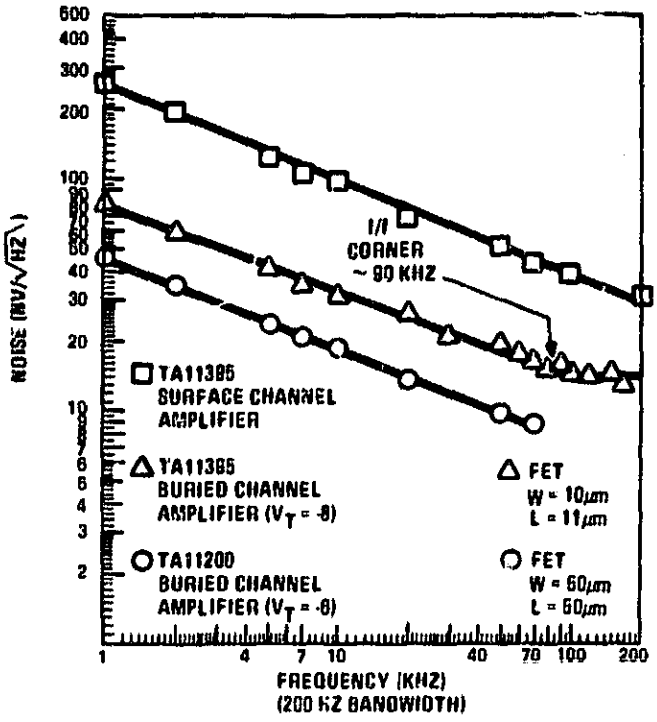
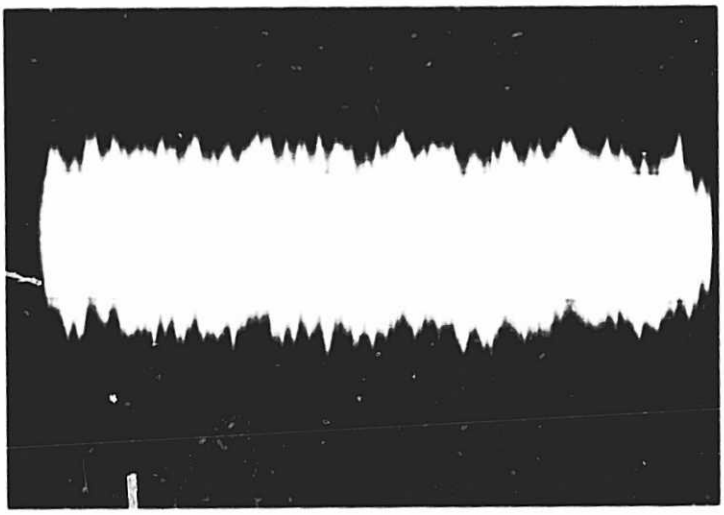


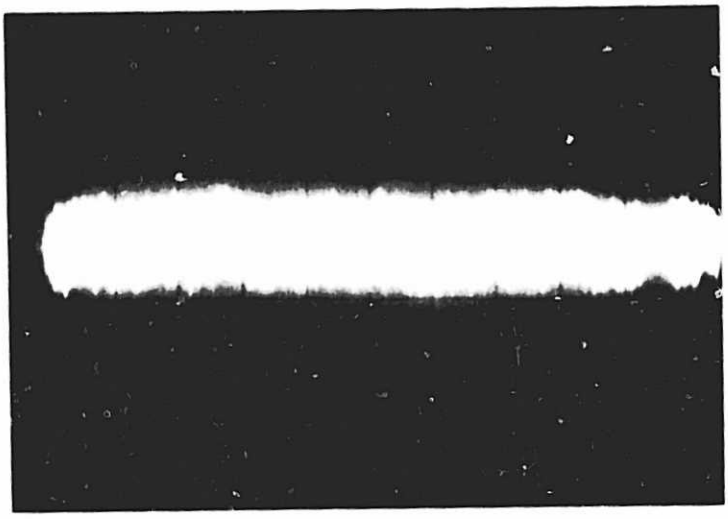
Fig. 2-15. Noise spectrum of buried amplifier and surface amplifier.

The value of V_{BCCD} was measured as 0.16 mV (see Fig. 2-14b). The resultant V_{ne} is therefore 0.23 mV. The additional noise is due to impedance effects at the input. Similarly, the noise output measured at 14.5 V, Z_{IN} = 10K is 0.18 mV which is 0.008 mV larger than V_{ne} which is calculated to be 0.172 mV. Thus, there is an increase in the noise level as the input impedance increases. This same effect is evident in the SCCD FET amplifier. The operational noise level of the BCCD amplifier, in the clocked floating diffusion reset mode, is the focus of another noise investigation currently in progress.

The conclusion to be drawn from these measurements is that a single-stage CCD FET on-chip amplifier provides lower noise performance than a two-stage enhancement FET on-chip amplifier. The voltage gain (A_V) for the buried-channel FET on the TA11395 was evaluated. The FET was configured as a source follower amplifier for all the operating modes that were investigated. The buried-channel FET has a gate width of W = 10 μm and a gate length of L = 11 μm. The source follower transfer characteristics for two values of source resistance (R_S) are shown in Fig. 2-19. A maximum linear range of 7.5 to 11 V is obtained for R_S = 20 kΩ. The gain for this value of resistance is A_V = 0.624 at room temperature. This linear range is compatible with the nominal CCD operating potentials. This may be seen by examining the floating diffusion and CCD channel potentials displayed in Fig. 2-14.



a. SCDD noise amplitude.



b. BCCD noise amplitude.

Fig. 2-16. Amplifier temporal noise.

a. SCCD noise amplitude.

b. BCCD noise amplitude.

Fig. 2-17. Band-limited amplifier temporal noise (1 kHz to 1 MHz).

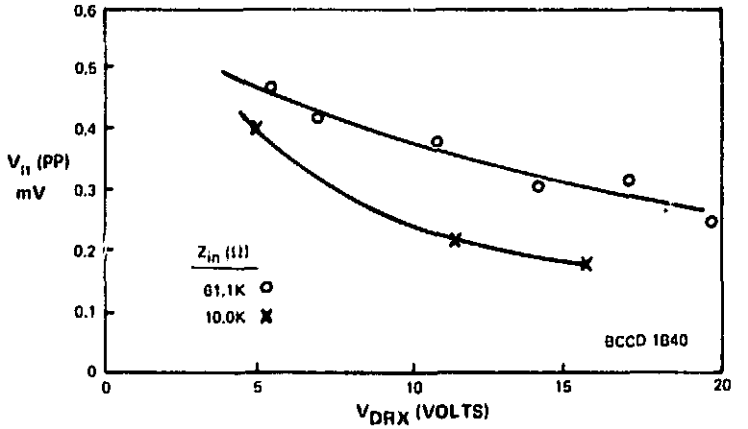


Fig. 18. BCCD amplifier noise.

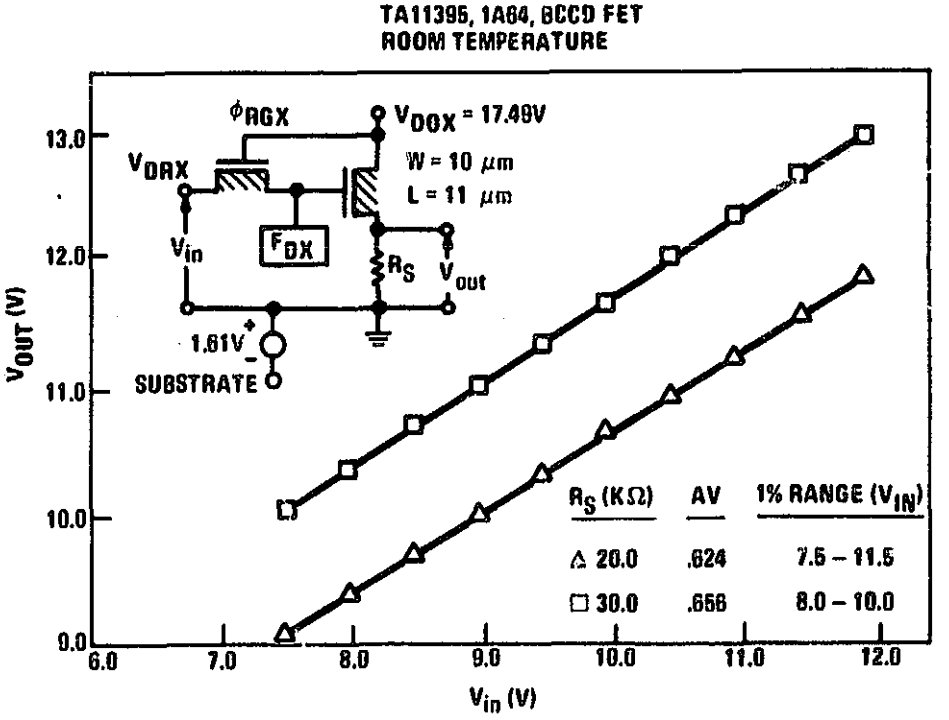
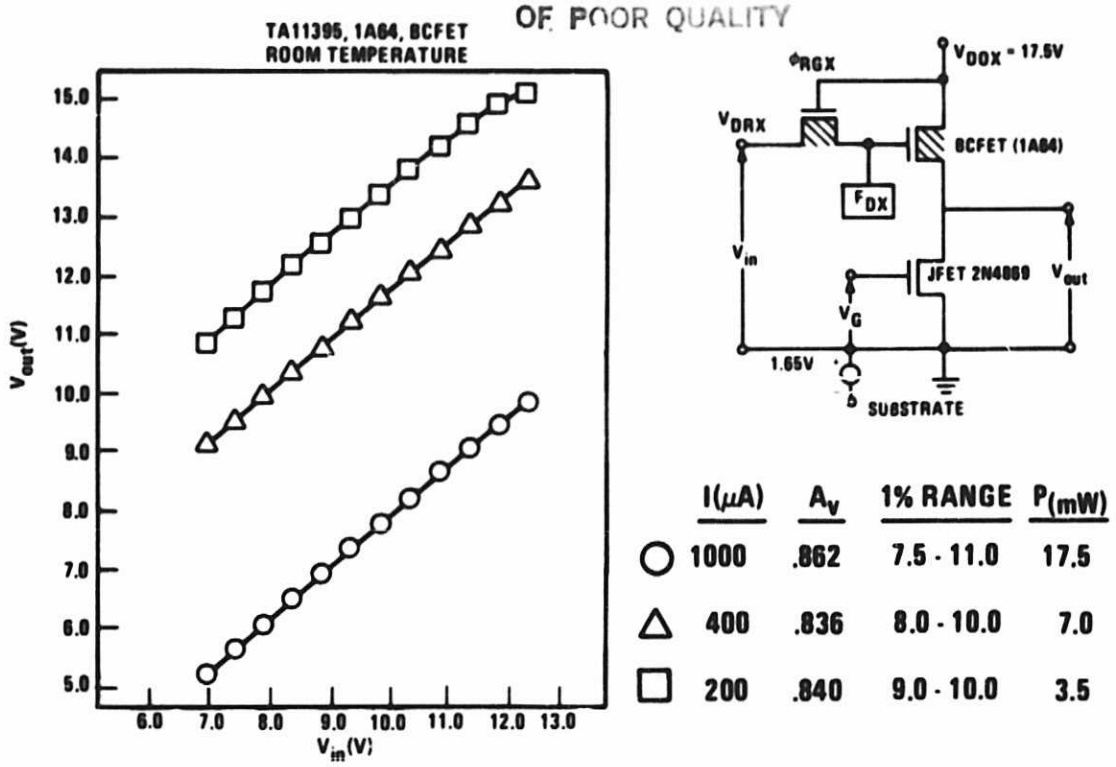


Fig. 2-19. Buried-channel FET source follower amplifier linearity.

The on-chip power consumed by the amplifier with the 20-kΩ resistor is 8.9 mW. In an effort to reduce this consumption a circuit was tested using a JFET (2N4869) as a constant current source load for the BCFET. It was expected that with the high R_{DS} of the JFET lower power and high gain would be achieved, while the constant current would help maintain high linearity.

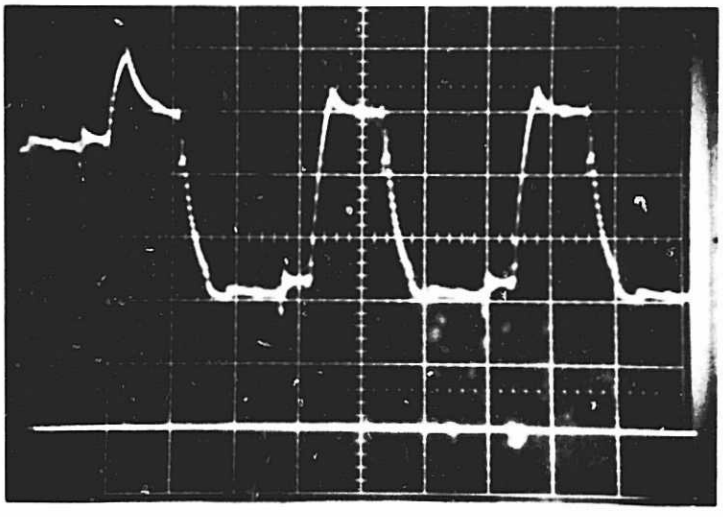
The circuit configuration with the JFET load is shown in Fig. 2-20. Plotting the voltage, V_{OUT} across the JFET load with three values of load current as a function of applied BCFET gate potential, V_{IN} results in the graph of Fig. 2-20. With 400 μA of load current an adequate linear range of 8 to 10 V was obtained while reducing the power consumed to 7 mW. The gain increased to A_V = 0.836. Investigation of the JFET load will be continued.



	I(μA)	A_v	1% RANGE	P(mW)
○	1000	.862	7.5 - 11.0	17.5
△	400	.836	8.0 - 10.0	7.0
□	200	.840	9.0 - 10.0	3.5

Fig. 2-20. Buried-channel source follower amplifier linearity with current source.

A typical output waveform from the BCCD floating diffusion amplifier may be seen in Fig. 2-21. This output structure does not have a dc isolation gate between the reset drain and the floating diffusion. The register is operating at a 300-kHz rate, corresponding to a dual-band module frame time of 1.8 ms. The load resistor is 10 kΩ.



200 mV/DIVISION 1 μs/DIVISION

Fig. 2-21. Typical output waveform from the BCCD floating diffusion amplifier.

Section 3

SCHOTTKY BARRIER IRCCD (Pd_2Si) PROCESS DEVELOPMENT

3.1 INTRODUCTION

Monolithic, 32-x-64, interline transfer Schottky barrier (SB) IRCCDs using thin palladium-silicide detectors, which are sensitive in the 1- to 3.5-μm spectral band, have been developed as process test vehicles for the SWIRS technology development.

The main advantage to using the silicon Schottky barrier IRCCD sensor technology is that these monolithic IRCCD arrays are fabricated using standard integrated circuit silicon technology and standard LSI processing techniques. Therefore, it is possible to construct blemish-free area and line arrays with high-density designs and large numbers of elements (>8000). In addition, Schottky barrier focal plane arrays (FPAs) have considerably higher photoresponse uniformity than that achieved by other FPA detector technologies; typically, nonuniformity is below 1%.

A process for the fabrication of thin-film (20 to 200 Å) Pd_2Si detectors with varying optical cavity dielectrics is under development. The effect of changes in process parameters (film thickness, dielectric thickness, heat treatment) on the detector sensitivity, dark current, and CCD transfer efficency are the subjects of this discussion.

3.2 Pd_2Si DETECTOR AND FPA TECHNOLOGY DEVELOPMENT

Our effort is aimed towards developing a high-yield process for the fabrication of Pd_2Si FPAs. These arrays and the individual Pd_2Si detectors are optimized for highest quantum efficiency in the 2.2-μm SWIR band and lowest possible dark current consistent with the radiometric accuracy required by the specifications (6 nA/cm^2 at 120°K and small reverse bias). An effort in the characterization of the 1/f noise characteristics as a function of guard ring doping, surface channel implant, and heat treatment cycle is now being launched.

3.2.1 Fabrication Yield and FPA Characterization

The fabrication yield and FPA characterization effort utilized the 32 x 63, TC1247 array mask set. Figure 3-1 illustrates the interline transfer organization of this IRCCD. The important achievements in this effort are:

- Reduction of the average black-spot density due to alteration in the heat treatment and etch procedures of the Pd_2Si detectors.
- Improvement in thickness control on Pd_2Si films.
- Elimination of CCD yield loss due to Pd residues on the wafer. This was achieved by introducing several redundant etch steps, after the detector formation.

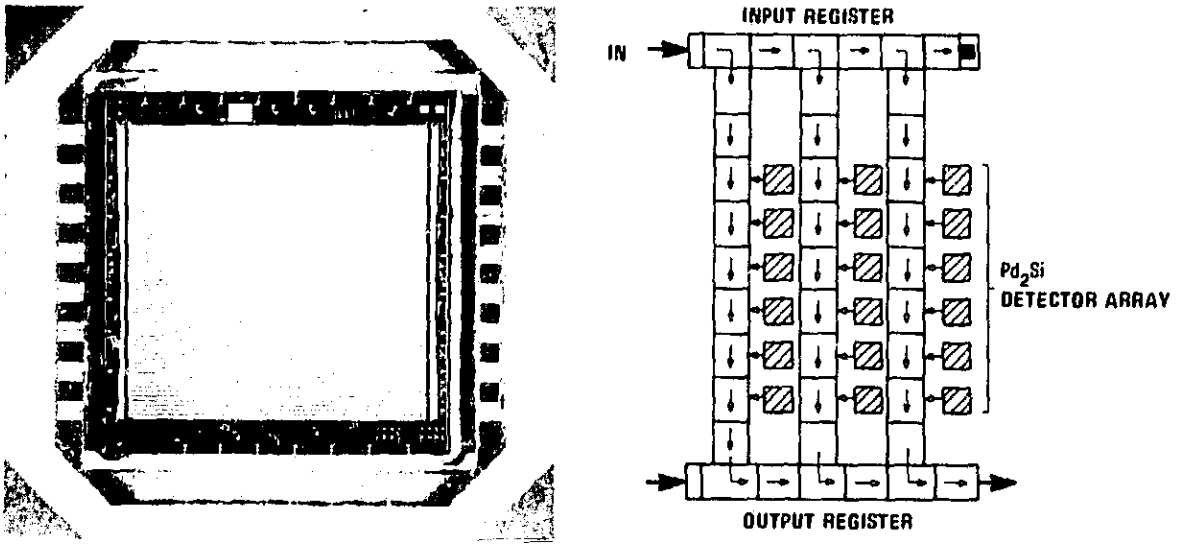


Fig. 3-1. Interline transfer.

- Elimination of the aluminum adhesion problem, i.e., the adhesion of Al pads to the oxide surface of the chip due to residues of Pd on the oxide. This problem limited the chip bonding yield.
- Realization of the effect of Pd_2Si detector heat treatment cycle on the transfer efficiency of the CCD. It was determined that high anneal temperatures degrade the low-light-level performance (without fat zero).
- Two good quality 32-x-63-element Pd_2Si arrays were delivered to J. Lorance at Princeton University for independent evaluation.

3.2.2 Optimization of Pd_2Si Detector Sensitivity

The optimization of Pd_2Si detector sensitivity used the test diode mask set TA13473. This mask set provides a 35-mil diameter circular detector structure with a guard ring, an optical cavity dielectric, and an aluminum mirror reflector (see Fig. 3-2).

The quantum efficiency is also measured on test detectors fabricated on the TC1247 array mask set (along side the actual 32-x-63-element array). This test device is shown on Fig. 3-3 and is approximately 520 mil^2 in area.

All quantum efficiency measurements are performed against a 1000°C black-body source with 0.5-inch aperture diameter. The radiation is incident on the detector

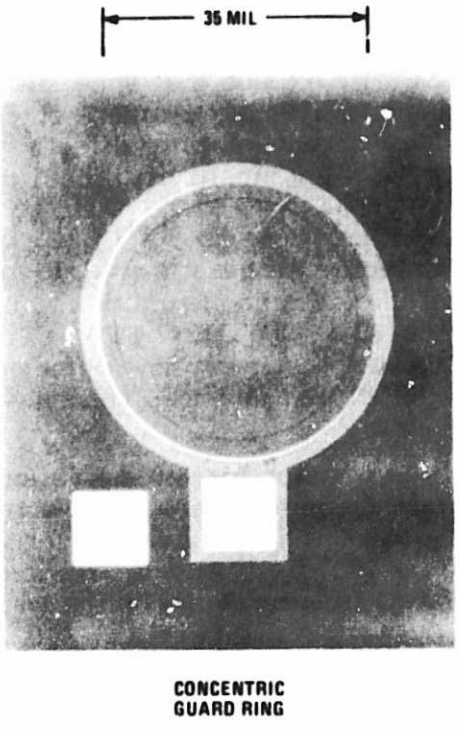


Fig. 3-2. Detector structure.

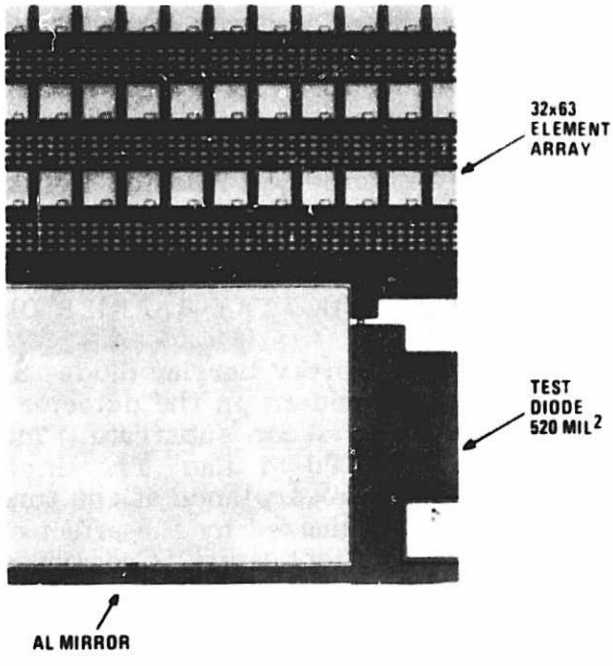


Fig. 3-3. Test device.

through a filter wheel and a barium-flouride window. The detectors are approximately 16 cm away from the black-body aperture. We do not correct for reflections on the front surface of the window, but we do correct for reflections on the front surface of the filters. We expect that the effective FPA sensitivity would correspond to these quantum efficiency unless the low-light-level CCD performance is degraded by some fixed trapping effects. The main achievement of this effort is identifying three high sensitivity Pd_2Si detector processes (see Fig. 3-4).

- The 15I/15V-type A detector process is a high-temperature process that yields a diffused silicide-silicon junction. This detector process was implemented on the 32-x-63 TC1247 FPA. The resulting arrays have practically no black spots, very low defect density up to 15 V net bias on the detectors, and less than 0.4% white spots above this bias.
- The 14B/11G/L36-8 type C detector process is an intermediate temperature process which was implemented on 32-x-63 TC1247 FPA. The resulting arrays had good low-light-level performance, but with high average black-spot density, typically $\sim$0.75%, and the FPA sensitivity varied by a factor of two from one side of the wafer to the other.
- The 2T/15P/14L type C detector process is a low-temperature process that yields an abrupt silicide-silicon junction. Our effort will be focused on the further development of this high-sensitivity process with a tuned optical cavity.
- The development of an alternate (FPA) process that calls for completing the CCD registers fabrication including Al contact sinter before the fabrication of the on-chip Pd_2Si detectors. This aluminum contact sinter process will improve the ohmic contact to diffusions and polysilicon gates and reduces the 1/f noise in the output amplifier. This process calls for covering the CCD array with etch resistant dielectric before forming and etching the Pd_2Si detectors. This process is currently under development. Independent measurements of the noise floor on Pd_2Si chips delivered to Princeton University suggest that this noise floor is 140 electrons (CDS processed noise). This floor may be acceptable without the need of this special FPA fabrication process.

3.3 PHOTORESPONSE OF Pd_2Si SCHOTTKY BARRIER DIODES

The structure of the Pd_2Si Schottky barrier diode (SBD) is illustrated in Fig. 3-5. The SWIR radiation is incident on the detector through a single-layer antireflection (AR) coating and the silicon substrate. The IR radiation is absorbed in the thin, 20- to 200-Å, Pd_2Si film. The single-layer AR coating results in a 30% increase in optical absorptance at the tuning wavelength. Optical absorptance in the Pd_2Si film is maximized by the effect of an optical cavity placed above the detector. The optical cavity is composed of a dielectric layer and an aluminum mirror. The proper choice of the dielectric layer thickness and index of refraction is essential to achieve the maximum improvement in sensitivity.

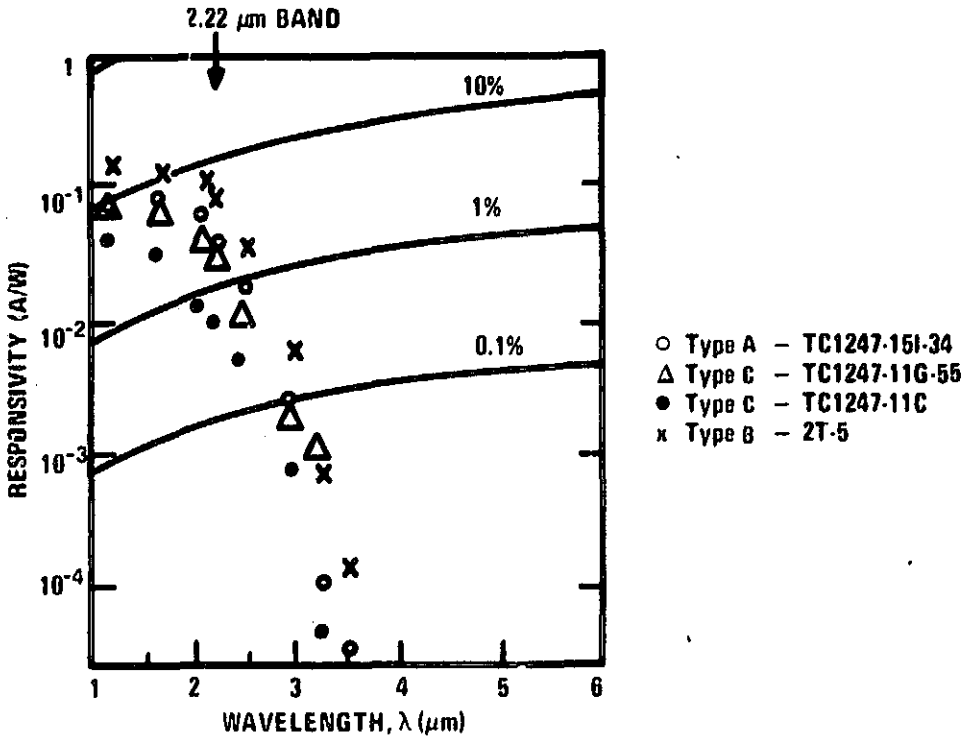


Fig. 3-4. Responsivity of AR-coated Pd_2Si detectors.

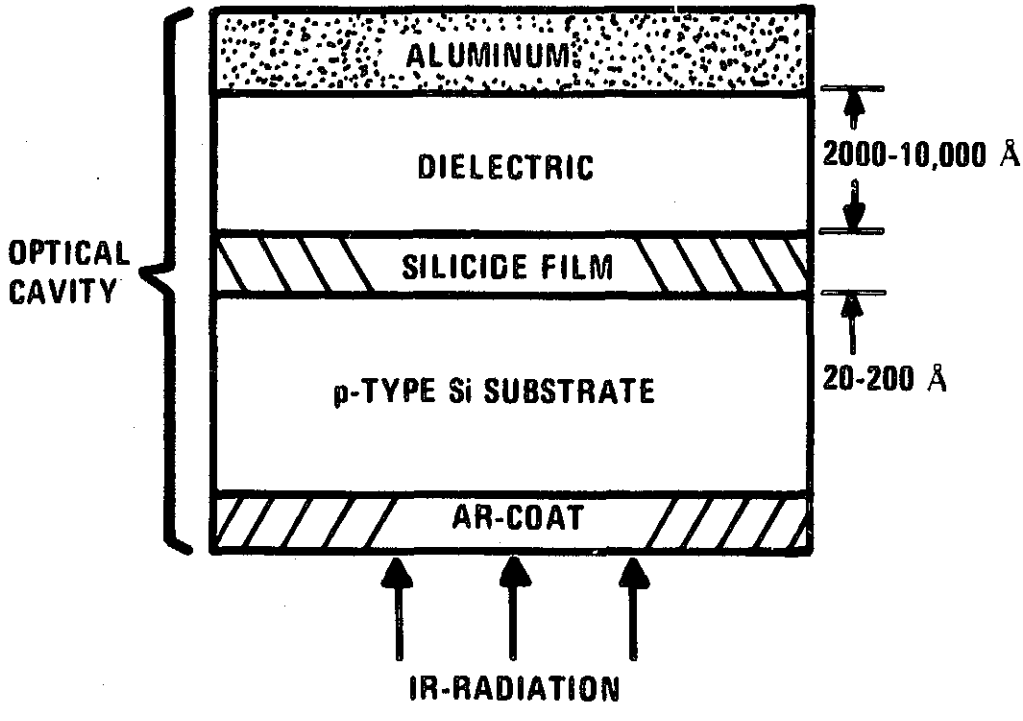


Fig. 3-5. Schottky barrier detector with optical cavity.

The photoresponsivity of two types of Pd_2Si SBDs is shown in Fig. 3-5. The type A Pd_2Si SBD corresponds to a diffused junction, whereas the type B Pd_2Si SBD is an abrupt junction with a near optimal thickness of the silicide layer. Both devices are fabricated with a tuned optical cavity and an AR coat. The sensitivity of type B SBD is twice that of type A. In our detector fabrication process, we aim at optimizing the photoresponse around 2.22 μm, to achieve a SNR equal to or larger than 110 with the Pd_2Si-IRCCD sensor at this band. Because the photoresponsivity of the Schottky barrier detector increases with higher photon energies, we expect considerably higher SNR at the 1.65-μm and 1.25-μm bands. The best quantum efficiency measured on single elements type A and B Pd_2Si-SBDs in the three SWIR bands is presented in Table 3-1. The average quantum efficiency measured on a wafer is somewhat lower than the best values reported here. The 15I and 15P devices were fabricated on a 32-x-63-element array, whereas the 2T device was fabricated on test diode structures.

3.3.1 Tuning the Optical Cavity

Optical transmission (T) and reflectance (R) measurements in the SWIR were conducted on thin Pd and Pd_2Si films on silicon. The absorptance (A) at 1.65-μm and 2.22-μm bands was computed from:

$$A = 1 - T - R \qquad (3\text{-}1)$$

where the reflectance is calibrated against an aluminum mirror. The absorptance of thin Pd_2Si films is plotted versus Pd_2Si film thickness, t, over the absorption length, $(1/\alpha)$ in Fig. 3-6. The 2.2-μm absorptance stays high over a wide range of Pd_2Si film thickness – between 0.5 to 1.5 times an absorptance length.

Thin Pd_2Si film absorbs more SWIR radiation than thicker films, $(t >> 1/\alpha)$; this is consistent with previously reported data.[10,11] The optical absorptance of Pd_2Si films on silicon were computed from fresnel equations. This calculated absorptance at 2.22 μm against Pd_2Si film thickness is also shown on Fig. 3-6. The index of refraction and the absorption coefficient, α, of thin Pd_2Si at 2.22 μm and 1.65 μm were determined from the absorption calculations that yields best fit to the data.

The calculated optical constants at 2.2 μm are used in determining the thickness of the cavity dielectric that will result in maximum optical absorptance in Pd_2Si films at 2.22 μm. The Pd_2Si detector responsivity is presented in Fig. 3-5 for types A; B SBDs have tuned optical cavity at 2.22 μm.

Tuning the optical cavity with a low index of refraction dielectric (type 2) results in a broad absorptance peak as a function of the thickness of the cavity dielectric in both the 1.65- and 2.22-μm bands.

TABLE 3-1. ANALYSIS OF PHOTOYIELD IN Pd_2Si — SBDs

Device (Type)	Junction Type	Dielectric Type	Wavelength								
			1.25μm 0.992 eV			1.65μm 0.752 eV			0.22μm 0.559 eV		
			A%	Y%	G	A%	Y%	G	A%	Y%	G
15I (A)	Diffused	Type 1	58.0	7.14	1.492	30.0	6.01	3.967	91.5	2.22	1.103
15P (B)	Abrupt	Type 1	62.0	11.0	2.151	13.0	4.0	6.093	71.0	2.68	1.716
2T (B)	Abrupt	Type 1	17.5	15.87	10.992	30.0	10.0	6.601	51.5	4.47	3.945
14B (C)	Diffused	Type 2	*	7.0	*	*	5	*	*	1.2	*
Design Goal				20			14			5.5	
Requirement to meet SNR				5.8			5.7			5.5	

*This process was fabricated and analyzed early in the program and these values have not been measured.

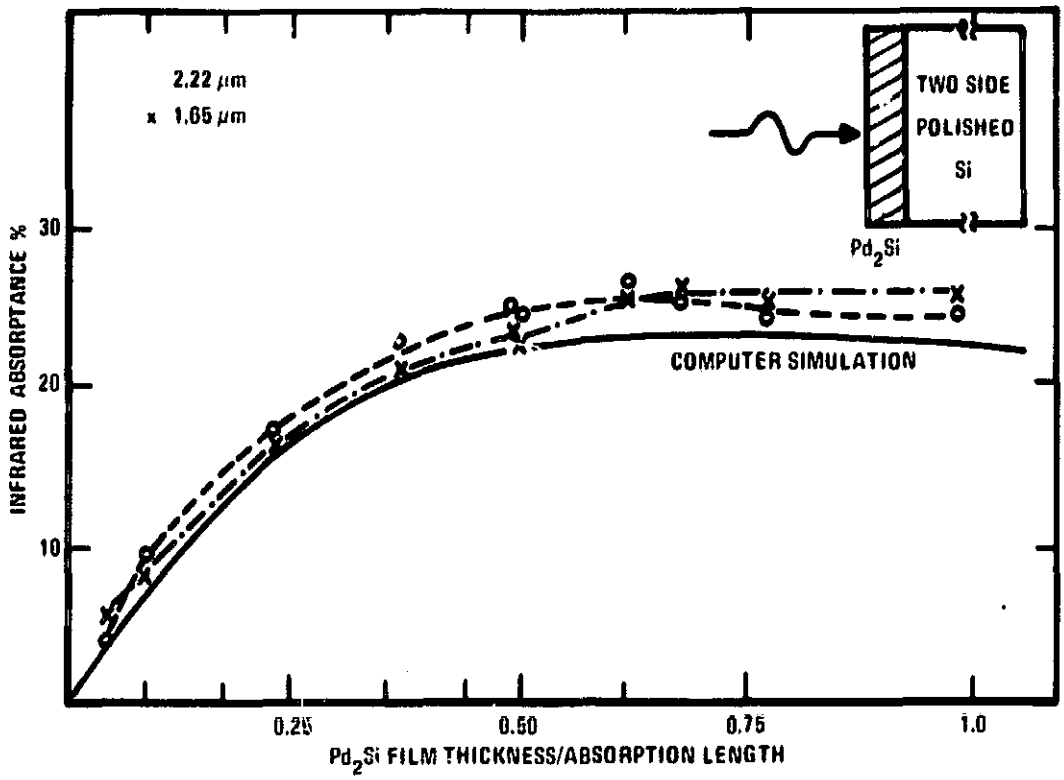


Fig. 3-6. Infrared absorptance in thin Pd_2Si films.

An example of this is seen in Fig. 3-7 and 3-8, where dielectric number 2 has a lower index of refraction than dielectric number 1. For the 14B devices at a given cavity dielectric thickness, the absorption in the 1.65- and 2.22-μm bands remains around 60%. By using the higher cavity dielectric index of refraction dielectrics (type 1) the magnitude of the absorptance changes between different spectral bands, as in the cases of 15I and 15P devices. The absorption characteristics of device 15P is undesirable. The cavity of the 15P device is mistuned and a resultant absorptance null occurs at 1.65 μm. The correct cavity dielectric thickness should retain relatively high optical absorptance in all SWIR bands. The thickness of the cavity dielectric number 1 required to tune the detector at 2.22 μm is smaller than the thickness of dielectric number 2 and hence easier to deposit uniformly.

Figures 3-9, 3-10, 3-11, and 3-12 demonstrate the absorptance nulls in PtSi and Pd2Si detectors. Figure 3-9 is a plot of PtSi photoyield versus photon energy for two PtSi detectors: 11H-75 and 12M-12. 11H-75 is a PtSi detector with type 2 dielectric whereas the 12M-12 represents a PtSi detector with a cavity tuned at 4.3 μm using type 1 dielectric. As can be seen on Fig. 3-9 and 3-10, optical cavity tuning enhances the photoyield and responsivity at the tuning wavelength but introduces some optical nulls at 1 and 2.2 μm. Figures 3-11 and 3-12 are plots of the photoyield and responsivity of type B Pd_2Si SBDs, 15P-40, and 2T-5. Detector 2T-5 represents a Pd_2Si SBD with cavity dielectric considerably thicker than that required to tune the cavity at 2.2 μm. As a result, an absorptance null at 1.65 μm is observed in the 15P-40 detector characteristic.

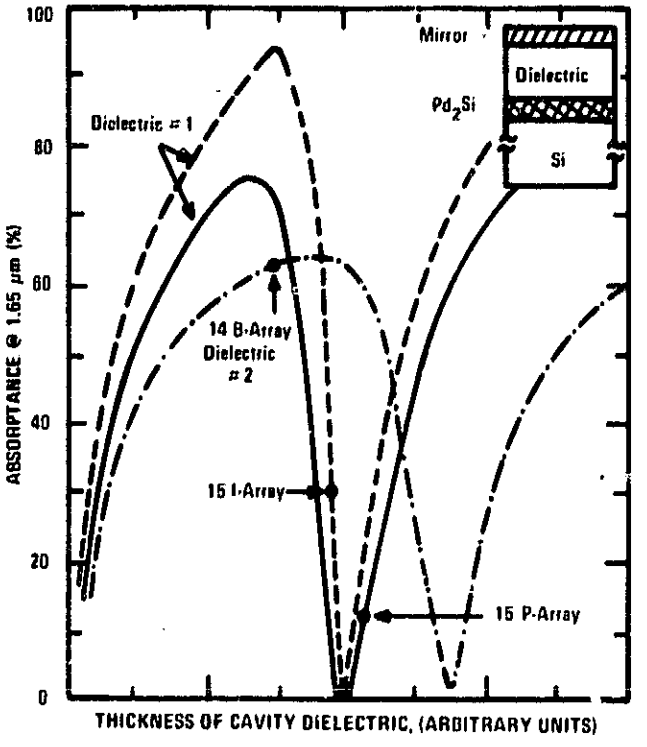


Fig. 3-7. Simulation of optical absorptance at 1.65 μm in Pd_2Si vs. thickness of cavity dielectric.

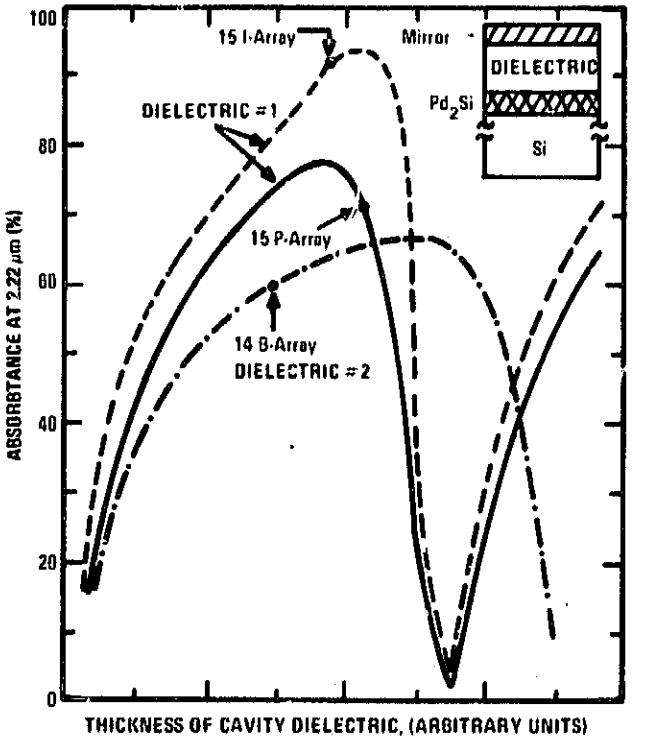


Fig. 3-8. Simulation of optical absorptance at 2.22 μm in Pd_2Si vs. thickness of cavity dielectric.

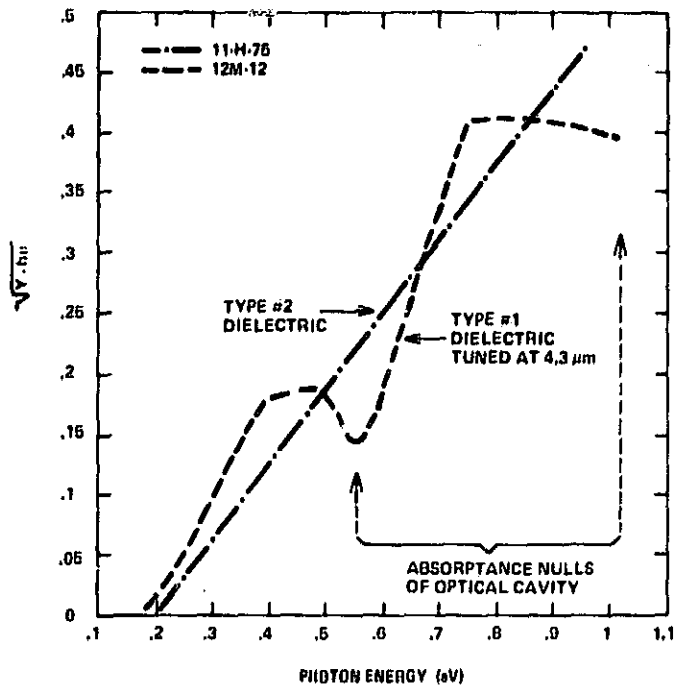


Fig. 3-9. Photoyield of PtSi Schottky barrier detectors with optical cavity.

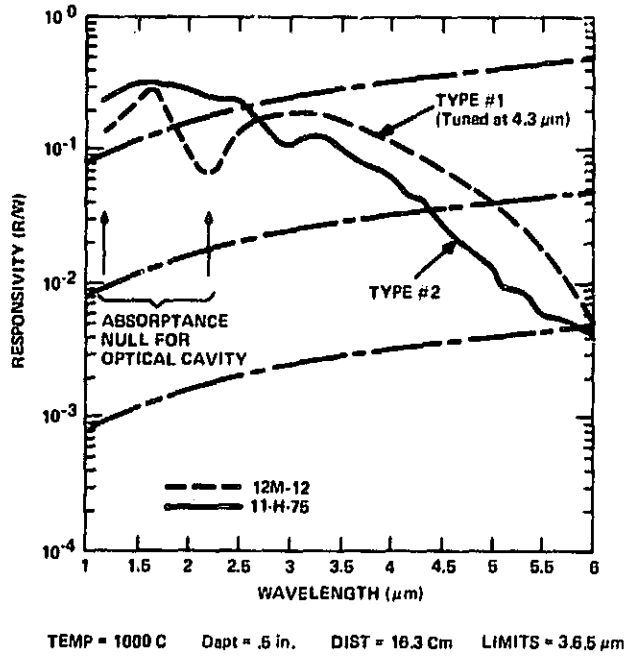


Fig. 3-10. Responsivity of PtSi Schottky barrier detectors with optical cavity.

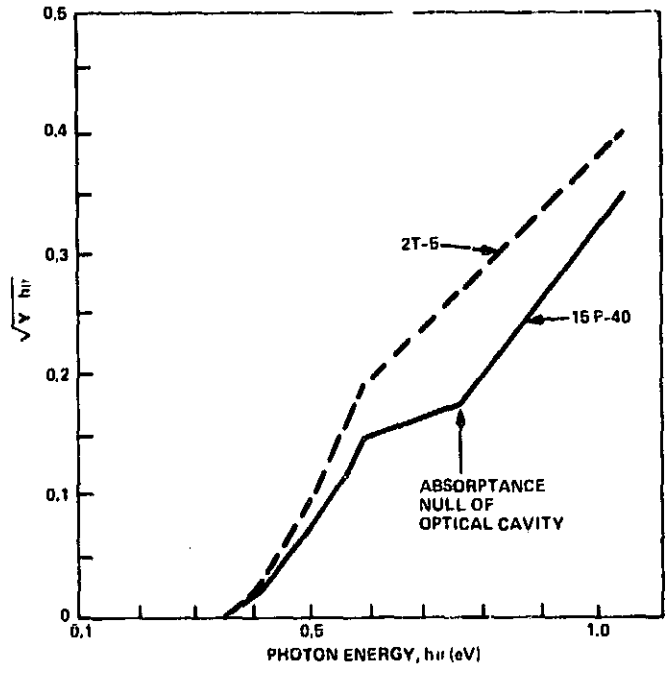


Fig. 3-11. Photoyield of Pd_2Si Schottky barrier detectors with optical cavity (type 1 dielectric).

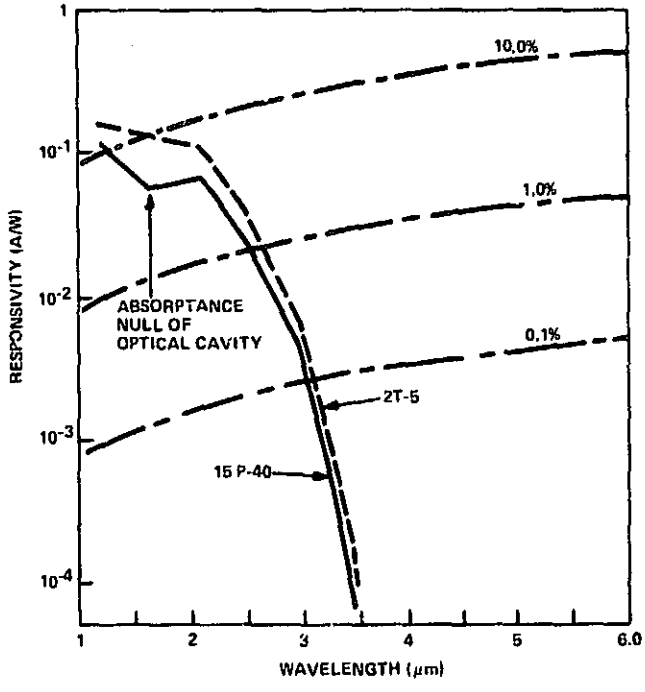


Fig. 3-12. Responsivity of Pd_2Si Schottky barrier detectors with tuned optical cavity (type 1 dielectric).

3.3.2 Responsivity Equations

The photoyield of an ideal Pd_2Si Schottky barrier detector is given by the following equations: [10]

$$Y(\lambda) = \frac{A(\lambda)\, G(\lambda)}{2} \left(1 - \sqrt{\frac{\Psi_{ms}}{h\upsilon}}\right)^2 \qquad (3\text{-}2a)$$

$$\simeq C_1 \frac{(h\upsilon - \Psi_{ms})^2}{h\upsilon} \qquad (3\text{-}2b)$$

where $A(\lambda)$ is the absorptance in the Pd_2Si at wavelength λ; $G(\lambda)$ is the internal quantum efficiency gain due to hot-hole scattering (reflection) at the silicide dielectric interface; Ψ_{ms} is the barrier height; $h\upsilon$ is the photon energy; and C_1 is the quantum efficiency coefficient.

The barrier height for Pd_2Si SBD is approximately 0.35 eV. The photoyield of thin-film Pd_2Si SBD in the three SWIR bands can be calculated by substituting photon energies from Table 3-1 into equation 3-2a.

$$Y(1.25) = 8.25\ GA\ (1.25\ \mu m)\% \qquad (3\text{-}3)$$

$$Y(1.65) = 5.05\ GA\ (1.65\ \mu m)\% \qquad (3\text{-}4)$$

$$Y(2.22) = 2.2\ GA\ (2.22\ \mu m)\% \qquad (3\text{-}5)$$

The quantum efficiency gain, G, is assumed to result from the scattering of hot-holes on the silicide film boundary. G is greater than or equal to unity and can be modeled by the following approximate equation:

$$G = 1 + \frac{n - e^{t/L} \sqrt{\frac{\Psi_{ms}}{h\upsilon}} \left(\frac{1 - e^{nt/L}}{1 - e^{t/L}}\right)}{1 - \sqrt{\frac{\Psi_{ms}}{h\upsilon}}} \qquad (3\text{-}6)$$

where

$$n = \frac{L}{2t} \ln\left(\frac{h\upsilon}{\Psi_{ms}}\right) \qquad (3\text{-}7)$$

and t is the thickness of the silicide layer, L is the attenuation length, and n represents the maximum number of chances that a hot-hole (with energy $h\upsilon$) has for emission into the silicon. [10] The solution to equation 3-6 as a function of L/t for Ψ_{ms} = 0.35 eV and λ = 1.25, 1.65, and 2.22 μm is shown on Fig. 3-13.

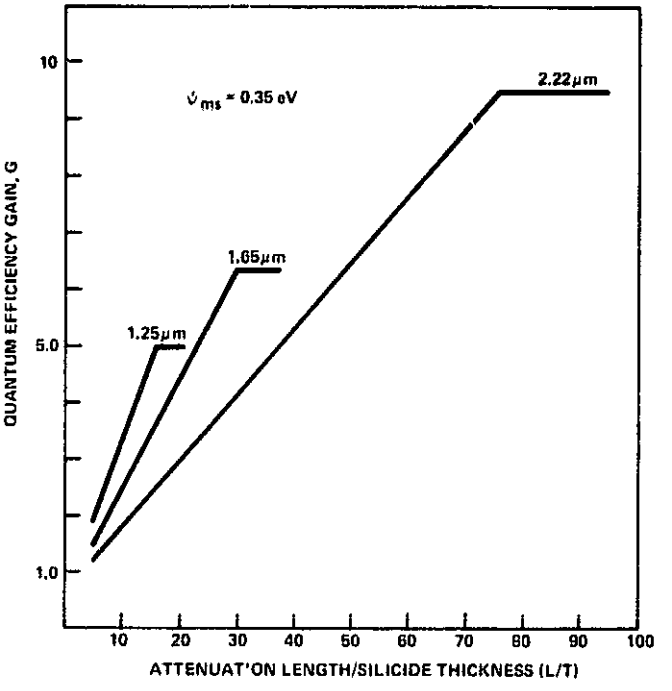


Fig. 3-13. Calculated quantum efficiency gain for Pd_2Si SBDs.

The theoretical limit on the quantum efficiency gain of a Schottky barrier detector due to surface scattering is given by: [10]

$$G_{max} = \frac{2}{1 - \sqrt{\frac{\Psi_{ms}}{h\upsilon}}} \qquad (3\text{-}8)$$

This corresponds to the condition when all hot-holes are emitted into the silicon. The maximum values of the quantum efficiency gains calculated from equation 3-8 are 9.5, 6.3, and 4.95 at 2.22, 1.65, and 1.25 μm, respectively. A multiplicative process is another quantum efficiency gain mechanism. It occurs when a hot-hole with high energy imparts part of its energy in a carrier-carrier collision to another hole. This may result in the emission of two hot-holes into the silicon for each high-energy photon absorbed.

Using equation 3-2a, the photoyield measurements conducted on Pd_2Si SBDs with various Pd_2Si layer thickness and the results of the calculations of optical absorptance, A, of Fig. 3-7 and 3-8 we calculate the internal quantum efficiency gain, G, as shown in Table 3-1. The process used in the fabrication of the 2T-type Pd_2Si detector results in the highest quantum efficiency gain and hence the highest photoyield in all three bands, in spite of lower optical absorptance.

The quantum efficiency gains calculated from the photoyield measurements are below the maximum gain values given by equation 3-8 in all bands except in the 1.25-μm band. For the 2T device, we compute a gain of 10.9 at 1.25 μm which is over twice the maximum value expected from equation 3-8 which is 4.95. The difference may be due to higher optical absorptance than calculated or a multiplicative process.

Also from Table 3-1, we observe that the photoyield of the abrupt junction detectors 2T and 15P at 2.22 μm is higher than that measured on the diffused junctions 15I. This is due to the optimization of the silicide thickness and the thinner interface region in an abrupt junction and hence a reduced probability of back scattering of hot holes at the interface.

3.4 DARK CURRENT CHARACTERISTICS

Measured dark current characteristics of thin PtSi and Pd_2Si SBDs as a function of operating temperature are shown on Fig. 3-14. The detectors are fabricated on N^-guard rings to avoid dark current spikes caused by excessive edge leakage. The measured dark current data are described by the Richardson thermionic emission model:

$$J_D = A^* T^2 e^{-q \Psi_{ms}/KT} \qquad (3\text{-}9)$$

where A^* is the Richardson emission constant for holes in silicon (ideally 32 A/cm^2K^2). The detector temperature is in °K, q is the electronic charge in

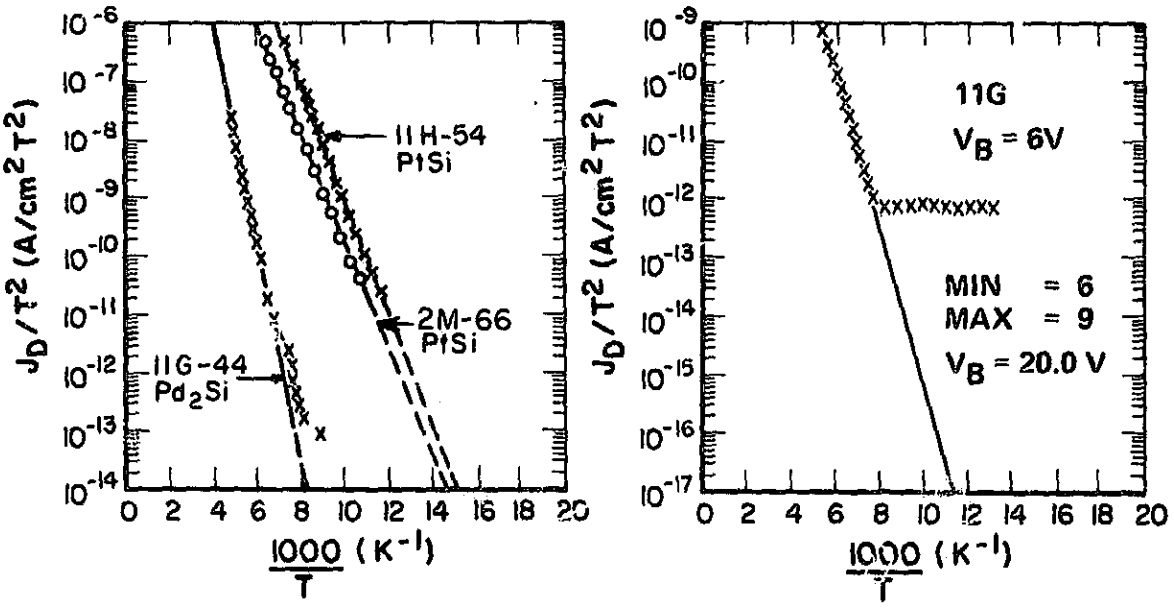


Fig. 3-14. Measured dark current characteristics for Pd_2Si and PtSi detectors.

coulombs, Ψ_{ms} is the activation energy or barrier height in eV, and K is Boltzmann's constant. The activation energy measured on the Pd_2Si 11G Schottky barrier detector is 0.37 eV; for PtSi it is either 0.18 or 0.2 eV, and hence a higher dark current density is observed for PtSi over Pd_2Si at any temperature.

The Pd_2Si single-stage CCD structure (see Fig. 3-15) was used in evaluating the effect of bias potential on the dark current activation energy and the value of the Richardson factor estimated from the thermionic model. The data are plotted on Fig. 3-16. The measurements show rapid decline in the activation energy between 0.35 and 0.29 eV when the detector bias changed between 4 V and 8 V. The value of A* also decreased from 1.2 A/cm^2K^2 to 0.25 A/cm^2K^2 over the same bias range.

The dark current density as a function of reversed bias voltage is shown in Fig. 3-17 for 11G type Pd_2Si detector at 130K. The dark current data illustrate a high reversed breakdown voltage, 34 V. The dark current density estimated on the 11G type Pd_2Si detector at 120K is around 2 nA/cm^2 at 5 V net reverse bias. From Fig. 3-17 we observe the same gradual increase in the dark current density with reverse bias, there after the dark current is constant above 11 V bias. The decline may be due to the Schottky image forces at the interfaces.

Shown also in this diagram are preliminary dark current measurements of the high-sensitivity 2T process. The data show an approximate increase in dark current by a factor of 2 over the 14B/11G process. These data, however, were taken with the parallel transfer gate biased at +20V and in actual practice this gate will be operated at a much lower bias. Dark current measurements at lower bias levels will be measured and it is expected the device dark current will be approximately equal to the 14B/11G process.

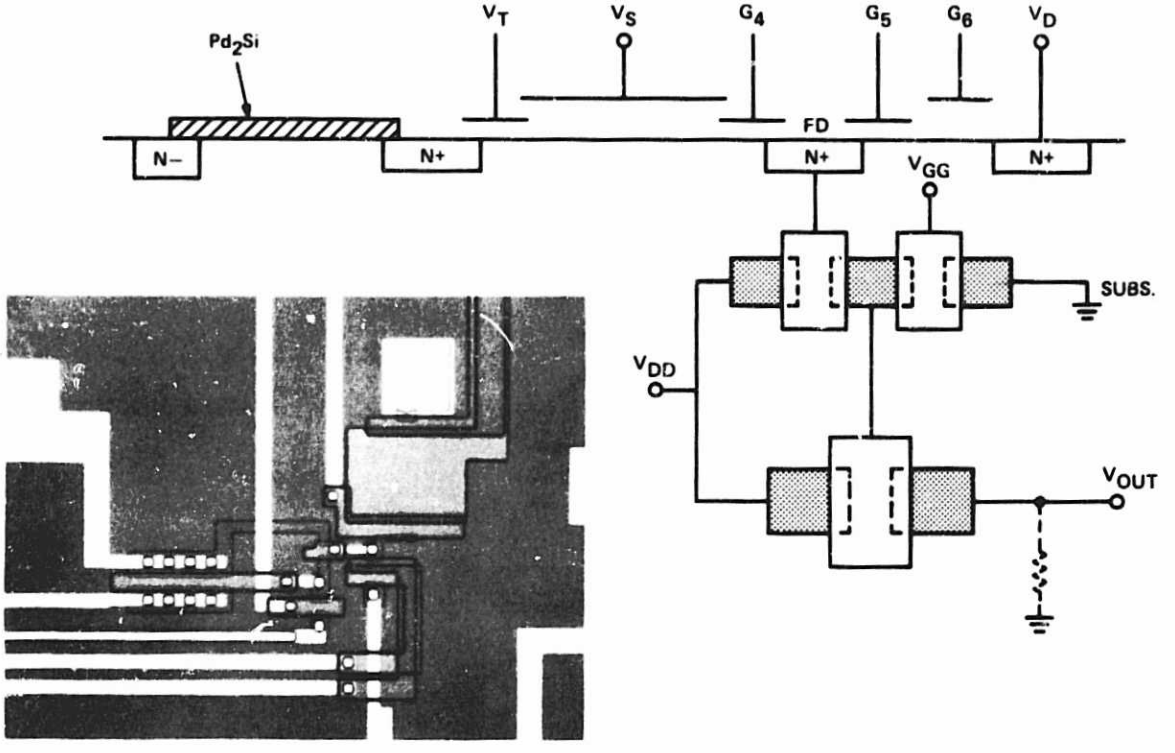


Fig. 3-15. Pd_2Si detector – single-stage CCD.

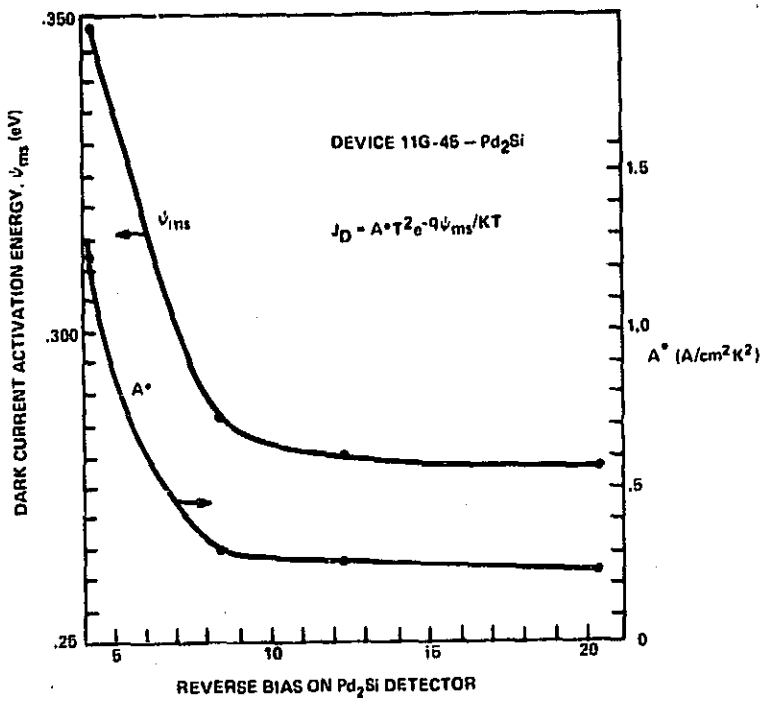


Fig. 3-16. The effect of reverse bias on the dark current characteristics of Pd_2Si SBDs.

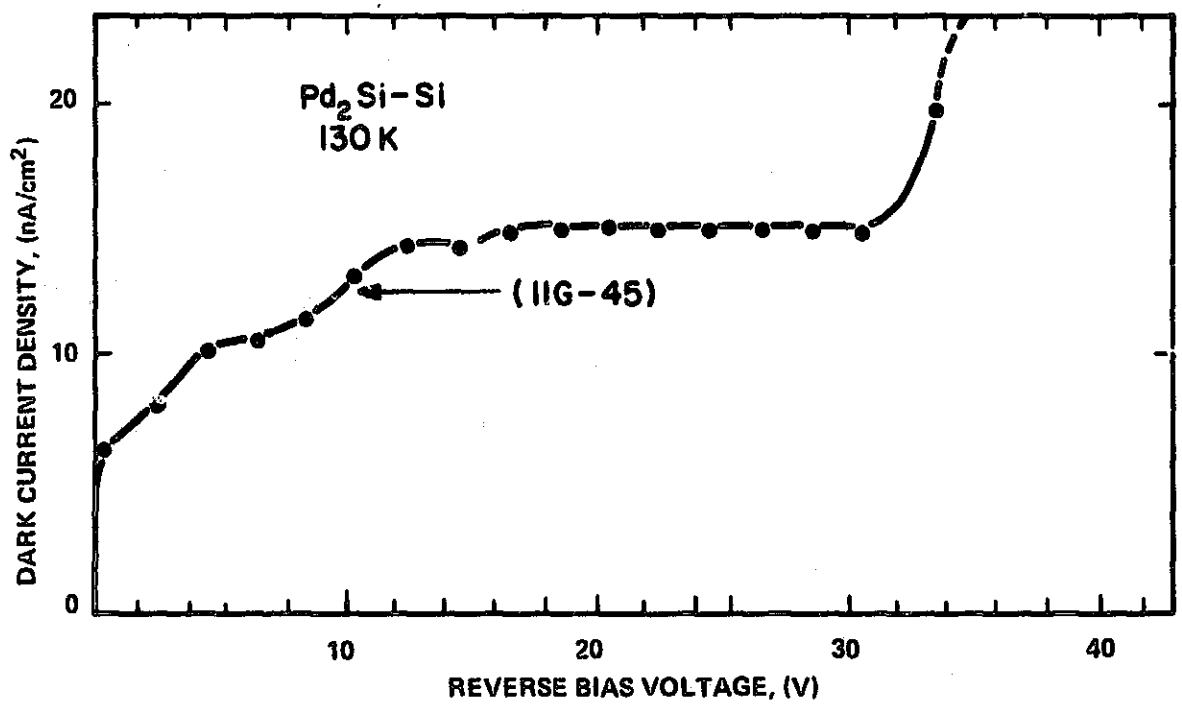


Fig. 3-17. Measured dark current density of Pd_2Si Schottky barrier detectors.

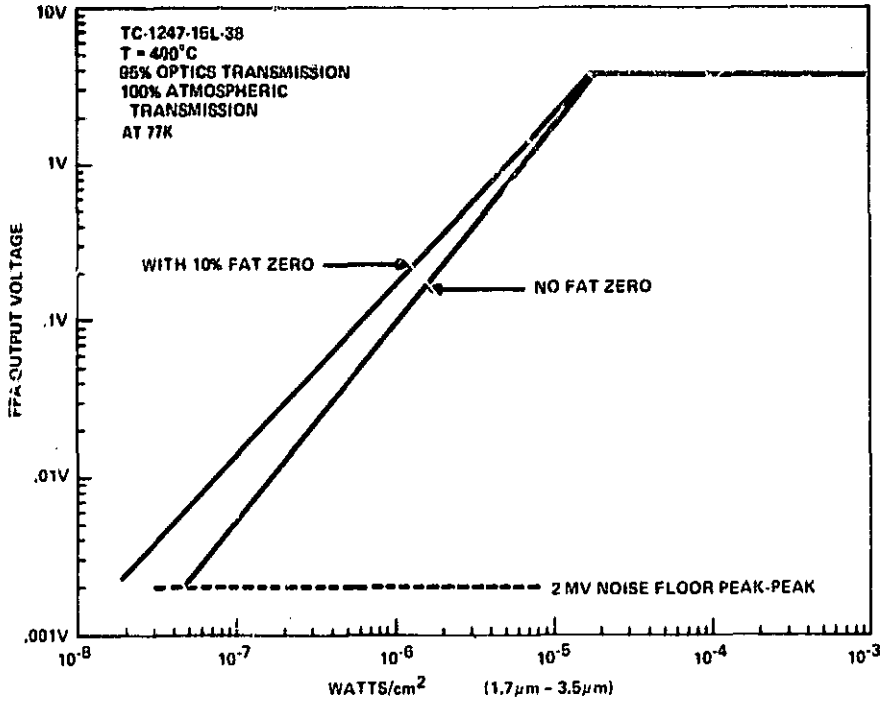


Fig. 3-18. Low-light-level signal output with and without fat zero.

3.5 TRANSFER CHARACTERISTICS OF Pd_2Si FOCAL PLANE ARRAYS (FPAs)

The transfer characteristic of Pd_2Si detectors was measured on the 32-x-63 series parallel series interline transfer FPA, with a 23 to 24% fill factor. The devices were operated with 60 frames per second and f/2 silicon optics. Imaging with Pd_2Si in the 1 to 3.5 μm wavelength region, results in no optical background signal. Therefore, the output voltage of the FPA corresponds to the optical signal and the dark current at the operating temperature.

The optical transfer curve of the 32-x-63-element IRCCD was measured on the 15L devices at 77K and is shown on Fig. 3-18. The detectors are read out in the charge reset or vidicon mode. The FPA was illuminated by a black body through neutral density filters and a square aperature. The image of the aperature corresponds to 5-x-5 pixels in the output video. The output voltage of the Pd_2Si FPA was measured at the center pixel in the aperture image. The responsivity of the Pd_2Si IRCCD is linear with incident radiation calculated in the 1- to 3.5-μm spectral band. The drop in the output voltage measured without bias charge compared to that with bias charge is indicative of a loss in the MTF due to trapping in the BCCD when operated without bias charge at 77K. The saturation in the output voltage corresponds to the maximum charge that the detector node capacitance can integrate under its bias conditions. In the vidicon readout mode, no blooming occurs when the device is illuminated with intensitives above the saturation intensity. The measured temporal noise, V_n, of the array in the dark is 2 mV p-p, or 0.65 mV rms.

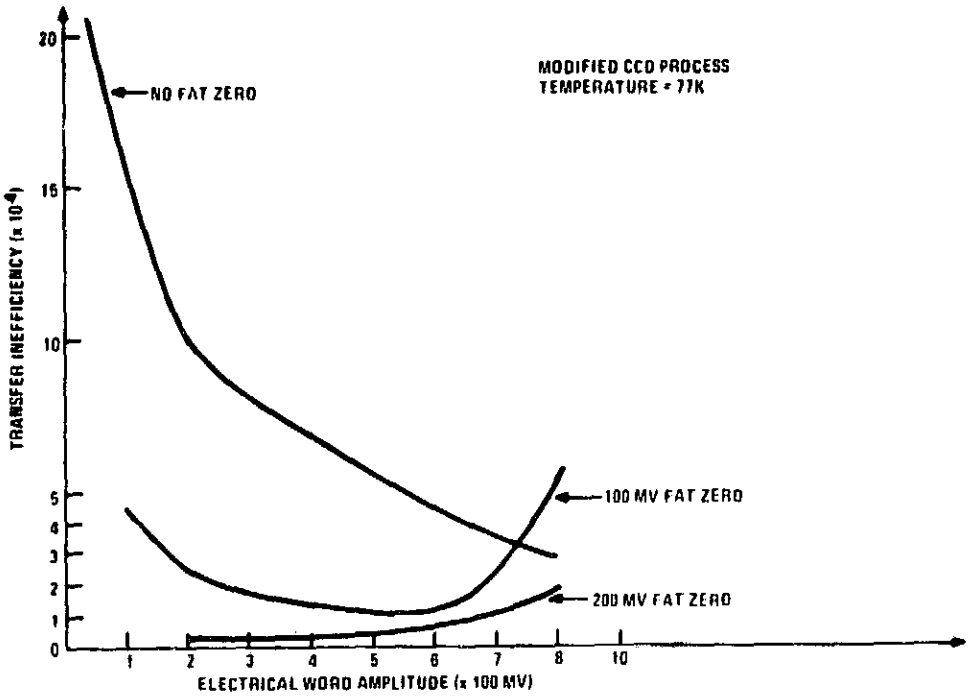


Fig. 3-19. Transfer efficiency measurements at 77K.

Actual transfer efficiency measurements have been made on the C-register of the 32-x-63 FPA. Figure 3-19 shows the transfer inefficiency measurements of the 14L device which has a modified C-register process aimed at decreasing the C-register transfer inefficiency. The 14L FPA has a channel length about 2.5 times longer than the TA11395 and the operating temperature of the 14L was 77K. (The transfer inefficiency of the TA11395 at room temperature is $\varepsilon = 3 \times 10^{-5}$). Both of these conditions for the 14L tend to degrade the device transfer characteristics. Figure 3-19 illustrates the increase in transfer inefficiency at low signal (light) levels at 77K. The transfer inefficiency (ε) improves considerably above 100K or with added bias change (fat zero). Shown in the figure is the ε reduction with the addition of a 100-mV and a 200-mV fat zero. The $\varepsilon = 5 \times 10^{-5}$ at a 600-mV signal with a 200-mV fat zero.

3.6 SUMMARY

The structure and the performance of the Pd_2Si Schottky barrier detector in the SWIR bands has been discussed. Improvement in the quantum efficiency of the Pd_2Si detector in the three SWIR bands was achieved by varying the thickness of the silicide layer, the thickness and the type of the cavity dielectric, and by forming an abrupt Schottky barrier junction in place of a junction with a diffused interface. Sensitivity measurements demonstrate also that the optical cavity when mistuned is capable of producing absorption nulls in the spectral band.

The dark current and the breakdown voltage of the Pd_2Si detector allows for operation of the IRCCD at intermediate temperatures of 120 to 145K, in either vidicon or charge skimming modes. Linear transfer characteristics is measured on the Pd_2Si IRCCD at 77K with vidicon mode detector readout.

Section 4

DUAL-BAND MODULE DESIGN

4.1 MODULE ARCHITECTURE

The dual-band module will consist of two linear detector arrays, with on-module CCD multiplexers and associated output amplifiers. The module will have a 30-μm center-to-center detector spacing. There will be one video output for each linear array; thus, there will be two signal outputs for each dual-band sensor.

It has been decided that the optimum number of detectors per band is 512. The module will thus have 1024 detectors. There is confidence in proposing this large number of detectors based upon the demonstrated yield in the Schottky barrier IRCCD technology. Of particular note is the fact that blemish-free 64-x-128 area arrays (>8,000 detectors) have been fabricated. Indeed, the Pd_2Si process test vehicle for the SWIR program has been the TC1247, a 32-x-64 area array (>2,000 detectors). Blemish-free TC1247 Pd_2Si imagers have been produced during the process development effort.

Two other array lengths were investigated, 256 detectors and 1024 detectors per band. The 1024-detector linear array was dismissed due to a number of factors. The primary reason for dismissal was the fact that a module with 1024 detectors per band would have a physical length of 1.2 inches. This chip length would reduce the number of complete die on a 3-inch wafer to less than 25. This is a number thought to be too low given yield considerations.

The 256-detector linear array was dismissed for two overriding reasons. First, a 256-detector array would have a length of 0.307 inch. This length is too short to readily accommodate the I/O connections to the Test Assembly hybrid. The nominal I/O requirements call for 22 bond pads per band and hybrid photolithography of 10-mil lines and 10-mil spaces. This dictates a module length of at least 0.440 inch. Thus, to accommodate a 2-x-256 module the hybrid photolithography and yield would be unduly taxed. The second reason for deciding against a smaller module is the increase in abuttment edges, bond wires, chip components, buffer amplifiers, and overall complexity associated with a reduction in the number of detectors per monolithic structure.

Two sensor architectures were studied (see Fig. 4-1). Both utilize a once per frame parallel transfer from the detectors to a serial CCD output register, which in turn transports the signal charge packets to a floating diffusion output amplifier. The first approach configured each band with the electrical input (used for set-up) at one end of the linear array and the video output at the other end. The direction of charge transfer for the entire serial output register is undirectional toward the output floating diffusion amplifier. The second approach placed the output floating diffusion amplifier at the center of the output serial register. The left 256 stages of the serial register transfer left to right toward the output, and the right 256 stages of the serial register transfer right to left toward the output. This second approach we call the center tap architecture.

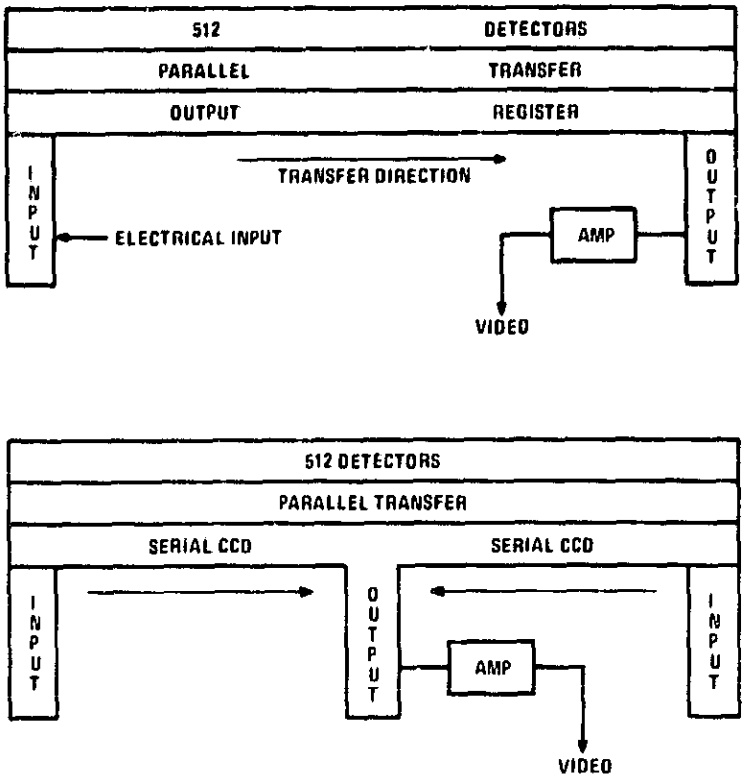


Fig. 4-1. Sensor architectures.

The center tap architecture was chosen for two reasons. First, the center tap configuration permits the maximum number of transfers between the furthest detector and the output to be reduced from (2/stage for two-phase operation) x (512 stages) = 1024 transfers to (2/stage) x (256 stages) = 512 transfers. This will reduce the transfer loss fluctation noise by a factor of $\sqrt{2}$ and improve the MTF of the device (the magnitude of these performance characteristics is discussed in a later section). Furthermore, the serial registers (left and right) each operate at one-half the clock frequency, compared to the unidirectional approach. The second reason for choosing the center tap architecture is that the floating diffusion output structure is placed in the middle of the chip, away from the butt edges. This permits unconstrained, minimum stray capacitance, optimized layout of the floating diffusion output structure and the NMOS amplifier. Furthermore, moving this sensitive electrometer (which produces 1 μV per electron) away from the damaged silicon edge should improve device yield. The unconventional output format is not considered to be a problem given that these devices undergo computer correction. The data format issue is discussed in the section on CCD output design.

A number of techniques were studied in deciding upon the optimum means of incorporating the center tap without a loss of pixels at the center tap location. This study proved to be useful in designing the electrical inputs for minimum pixel loss at the butting seams. The approaches for accommodating the center tap and the electrical input are detailed in Table 4-1. The first approach utilizes a 90-degree CCD channel turn-out of (into) the serial CCD register.

TABLE 4-1. TECHNIQUES FOR ACCOMMODATING INPUT/OUTPUT WITHIN 30-μm DETECTOR PITCH

Technique	Comments
90° Turn CCD Channel into Serial Register	• Layout of high-performance input/output difficult • Proven by Bell Northern
90° Turn with Resistive Gate into Serial Register	• Difficult to layout • Reliability suspect • Used by Philips
Corner Diffusion into Serial Register	• Some transfer efficiency degradation • Proven by RCA and TI
Fanned Parallel Transfer from Detectors to Reduced Pitch CCD	• Layout of high-performance input/output possible • No transfer efficiency problem • Used by Honeywell

This approach is generally quite good. However, for our parallel transfer design the layout of the clock bussing is very difficult, given that the device is fabricated in the two-level poly process with one level of metal. As an illustration of the technique, Fig. 4-2 shows a 90-degree layout for a simplified parallel transfer architecture, and simplified fill-and-spill input.

A second method is to utilize the resistive gate 90-degree CCD channel turn. This permits the input/output structures to be placed further away from the congested bussing areas. In this technique, charge transfer over extended distances is accomplished by applying a voltage differential along a polysilicon transfer gate. The voltage differential establishes an electrical drift field to transport the charge along the gate length. This technique has suspect reliability given the envisioned voltage differential along the resistive gate.

The third technique studied is the corner diffusion. The corner diffusion technique (see Fig. 4-3) utilizes two N^+ diffusions to couple CCD channels 1 to 15 mils apart. This technique has been utilized on RCA signal processing devices. The drawback to this technique is the transfer inefficiency at low signal levels (levels comparable to those seen in the 2.22-μm band). An expression for the transfer inefficiency is given by:

$$\varepsilon_{corner} = \frac{dQ_r}{dQ_s} = \left[1 + \frac{\beta(Q_b + Q_s)}{4 f_c C_{CD}^2}\right]^{-2} \qquad (4\text{-}1)$$

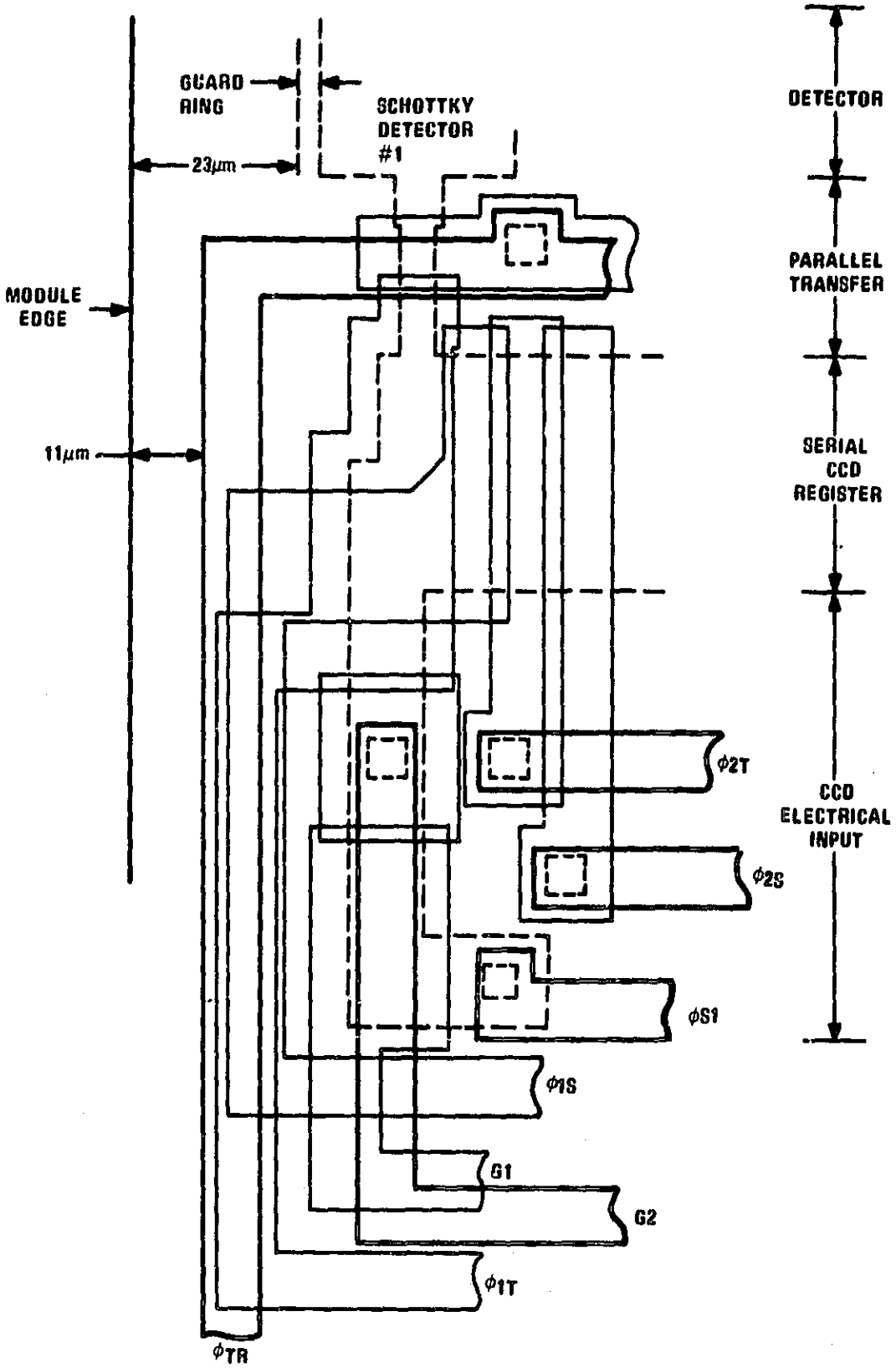


Fig. 4-2. Layout of electrical input.

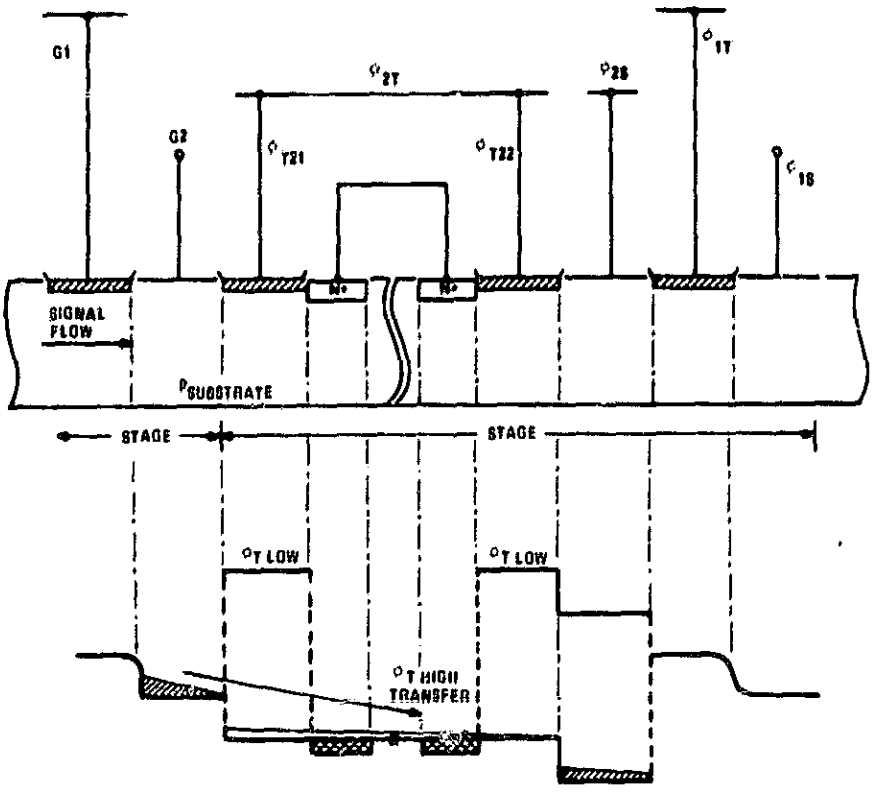


Fig. 4-3. Structure of corner diffusion and associated gate.

where $Q_b + Q_s$ is the charge, Q_r is the charge remaining, and f_c is the CCD clock frequency. C_{CD} is the corner diffusion capacitance, and B is the FET gain factor, $W_u C_i/L$. Here W and L are the FET channel width and length, u is the electron mobility, and C_i is the channel capacitance. The difficulty at low signal levels is the large decrease in the FET gain factor.

The fourth approach, and the one chosen for the dual-band sensor, is the fanned parallel transfer from detectors with reduced CCD serial register pitch. With this technique the serial CCD register is shortened from the detector 30-μm pitch to a 29-μm pitch for 35 stages at two places in the array and 20 stages at two other places in the array. The four locations are (1) at the left electrical input (35), (2) at the right electrical input (35), (3) at the left of the center tap (20), and (4) at the right of the center tap (20). The fan locations are shown in Fig. 4-4. By effectively moving the active CCD channel away from the butt edges (1 and 2) and the center tap (3 and 4), space is available to accomodate high-performance input and output layouts, and space is available for running buss lines. As will be discussed in the next section, the increase in transfer length between the detectors and the serial register is not expected to cause degradation in the parallel transfer operation.

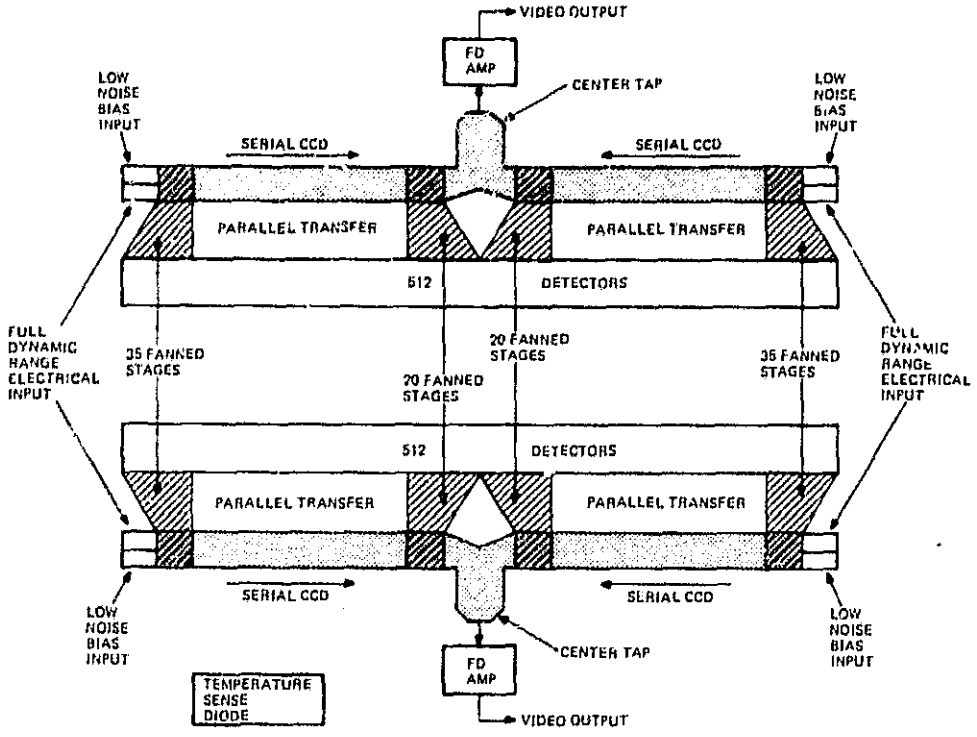


Fig. 4-4. Dual-band sensor architecture.

4.2 DETECTOR AND PARALLEL TRANSFER DESIGN

4.2.1 Parallel Transfer Region Design

The detector and parallel transfer region design provides versatility in imager operating modes and provides the ability to investigate different detector isolation techniques. Figure 4-5 shows a simplified parallel transfer design. The actual parallel transfer design incorporated in the dual-band sensor utilizes three parallel transfer gates instead of the conventional one-gate design. Figure 4-6 shows a first-generation layout of the three-gate transfer regions for both a fanned region and a straight region. The three-gate parallel transfer approach permits three modes of detector operation.

The first mode of operation is the continuous charge skimming mode. In this mode the first parallel transfer gate (ϕTR1) is kept at a constant DC bias. The second gate is either maintained at a DC bias, or is pulsed once per frame to enhance the parallel transfer. The third gate is pulsed once per frame to provide transfer into the serial register. The continuous charge skimming mode is depicted in Fig. 4-7a. The continuous charge skimming mode is analogous to the direct injection technique used with narrow band-gap semiconductors. The possible advantages of the skimming mode are reduced detector dark current and reduced 1/f noise.

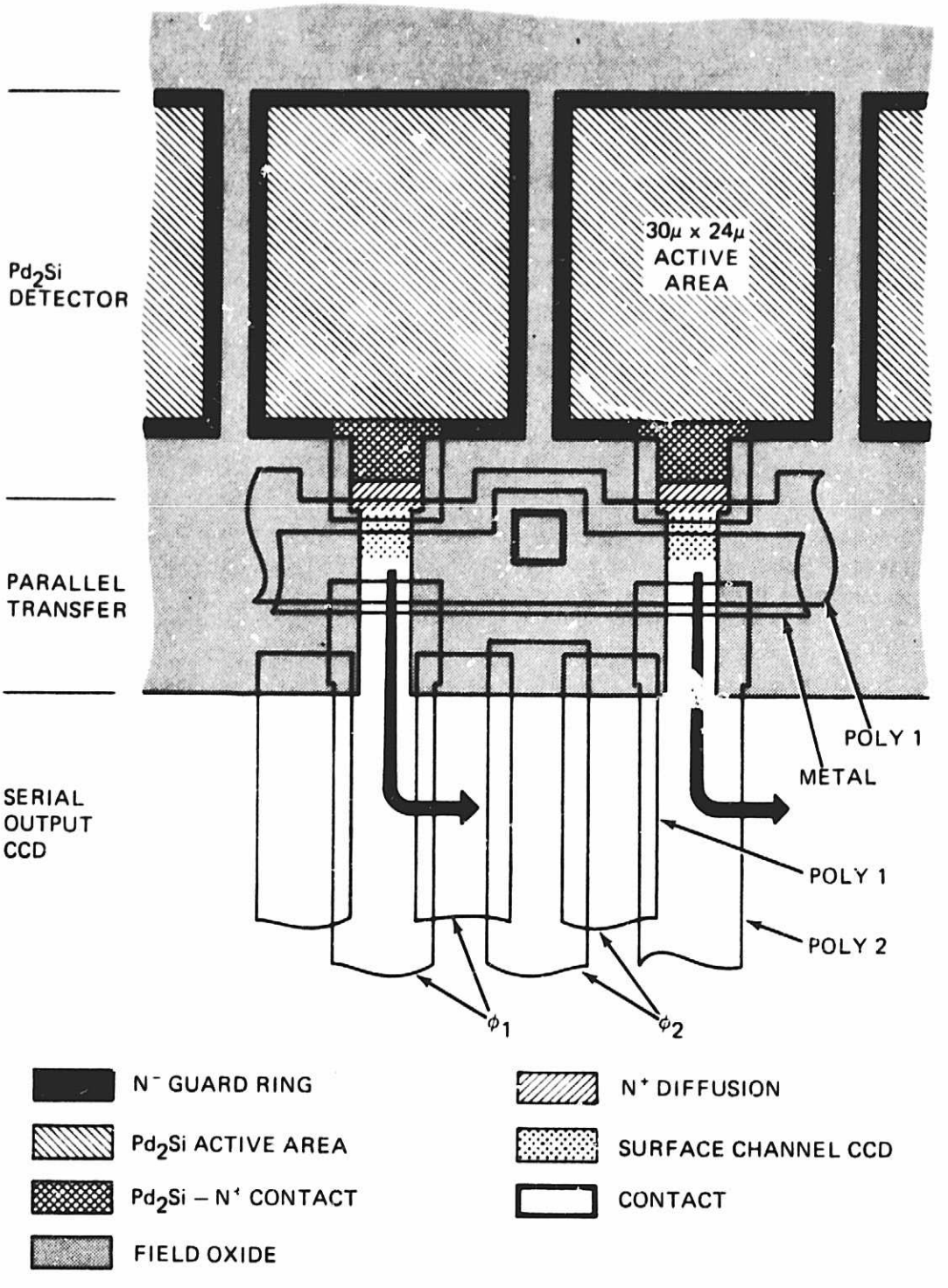


Fig. 4-5. Simplified detector, parallel transfer gate, and CCD serial register.

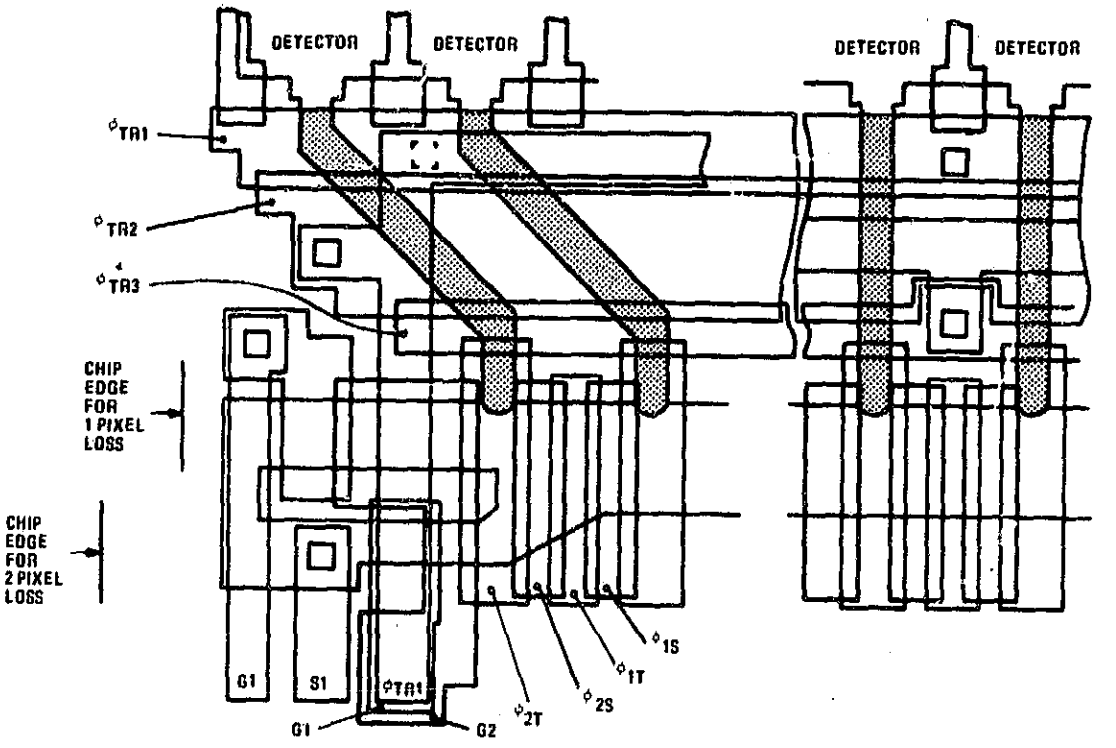


Fig. 4-6. Fanned parallel transfer layout.

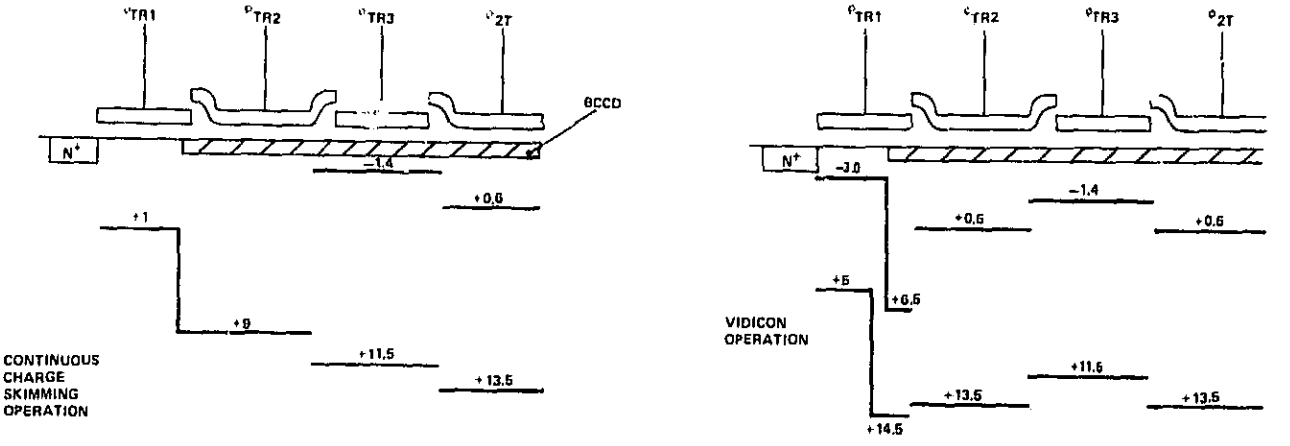


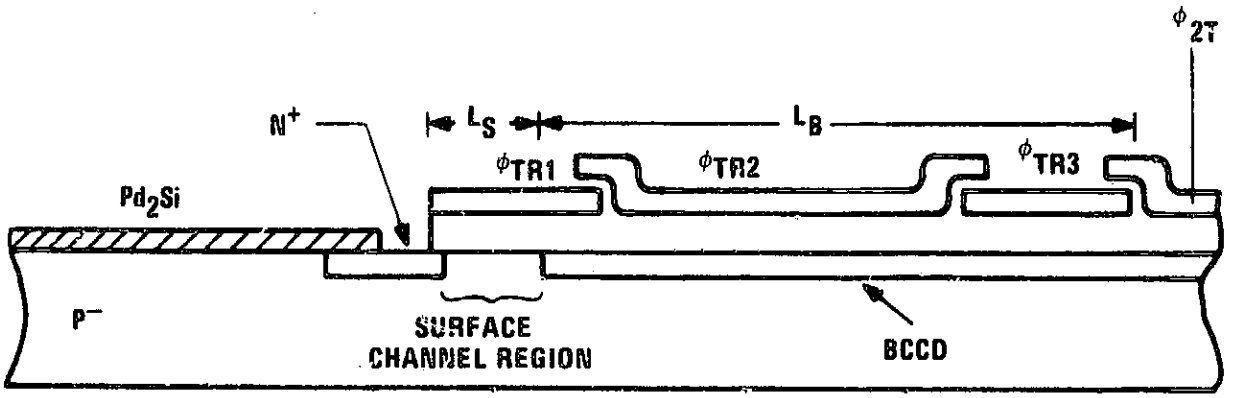
Fig. 4-7. Parallel transfer modes of operation.

The second mode of operation is the vidicon mode. This is the pulsed mode of operation utilized on the majority of the IRCCD imagers. This approach is the baseline method for operation of the dual-band sensor. Figure 4-7b depicts the clocking required for vidicon operation. In this mode all three parallel transfer gates are pulsed in a nested fashion to provide the once-per-frame transfer from the detectors to the serial register. The advantages of this mode are maximum transfer efficiency from the detector and inherent anti-blooming.

A third mode of operation is currently being studied. This mode will utilize the three gate parallel transfer structure in a novel, clocked sequence to hopefully provide enhanced low-light-level performance.

4.2.2 Parallel Transfer Region Dimensions

There were a number of design issues regarding the parallel transfer region (see Fig. 4-8). The design decisions were made based upon empirical evaluation of structures representative of the various design options. The first investigation involved the measurement of channel potential (V_{MB}) as a function of channel width. This measurement was necessary to assure minimal parallel transfer region trapping. It was found that the V_{MB} potential for the first level polysilicon channels decreases by 200 mV for a channel width change from 10 μm to 5 μm (room temperature measurement). The channel potential changes by 700 mV for a channel width change from 5 μm to 3 μm. The V_{MB}



DESIGN REQUIREMENT	COMPLETE CHARGE TRANSFER AND NO LAG
DESIGN ISSUES	SURFACE CHANNEL REGION DIMENSIONS (L_S, W_S)
	SURFACE CHANNEL REGION DOPING
	BURIED CHANNEL CCD GATE LENGTHS (L_B)
	BURIED CHANNEL CCD CHANNEL WIDTH (W_B)

Fig. 4-8. Parallel transfer region issues.

potential for second-level polysilicon channels decreases by 500 mV for a channel width change from 10 μm to 3 μm. The change in potential as a function of channel width is thus greater for the first polysilicon channels. The rate of change for the first polysilicon channels in the vicinity of 6-μm channel width is estimated to be 195 mV/μm. This degree of channel potential sensitivity combined with the details of the fan layout (the performance pacing layout) should pose no performance limitation. Therefore, the parallel transfer channel width was chosen to be 6 μm (both the surface- and buried-channel dimensions are 6 μm).

Another design issue was the effect of gate length on CCD transfer efficiency. Measurements were done to determine the degradation in CCD transfer efficiency for long transfer gate lengths. The conclusion from this investigation is that fan parallel transfer length and corner turning length of 20-40 μm pose no problem at the SWIR clock rates. This conclusion is based on measurements of performance of a TC1247 imager with 40-μm C-register gate lengths.

Table 4-2 details the parallel transfer design dimensions for the dual-band sensor. The maximum channel width and length occurs in the fanned regions.

TABLE 4-2. PARALLEL TRANSFER DESIGN DIMENSIONS

Channel Region	Effective Width (μm)		Effective Length (μm)	
	Max.	Min.	Max.	Min.
ϕ_{TR1}				
Surface	6	6	9	9
Buried	6	6	2	2
ϕ_{TR2}				
Buried	8	6	30	23
ϕ_{TR3}				
Buried	8	6	28	22
ϕ_{2T}				
Buried	6	6	9*	9

*Length computed to serial register edge.

4.2.3 Detector Design

The Schottky barrier detector consists of the aluminum reflector, the optical cavity dielectric, the silicide layer formed upon P type silicon, the N^+ output coupling diffusion, and a detector isolation structure. A cross section for a simplified structure may be seen in Fig. 4-9. The details of the optical cavity and the silicide layer design are discussed in the process optimization section. The N^+ coupling diffusion is the transport vehicle to couple the photogenerated charge and dark current from the silicide to the CCD parallel transfer region. The major issue for this discussion rests in the detector isolation design.

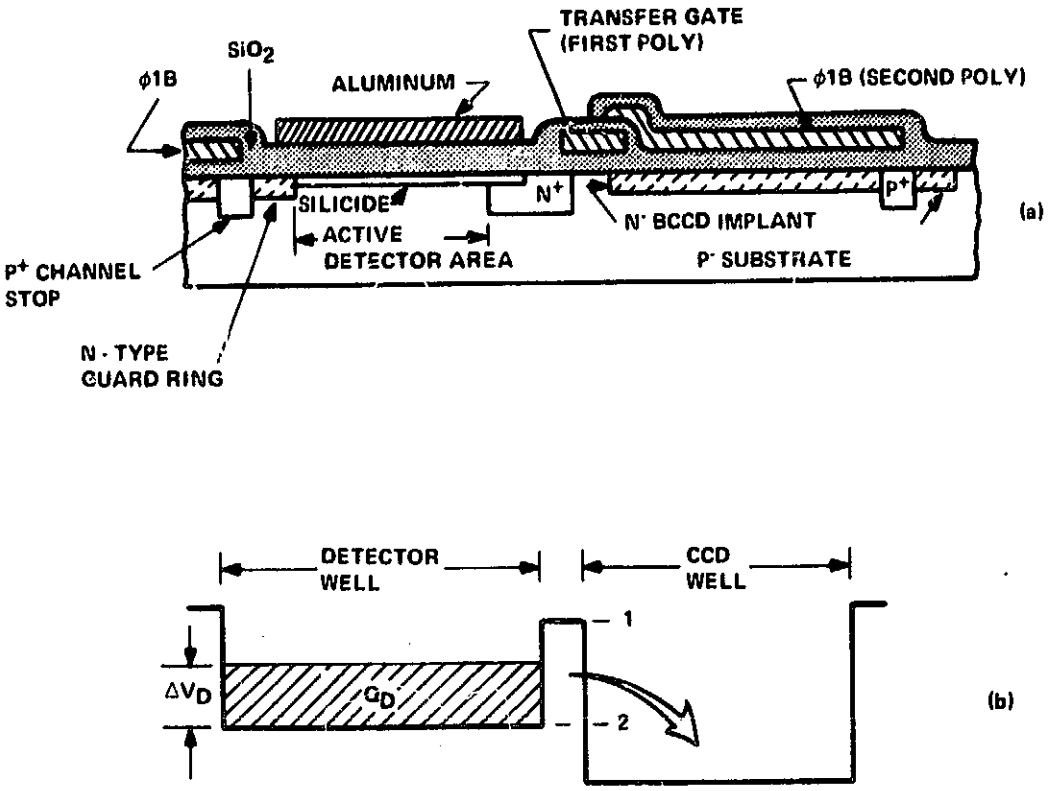
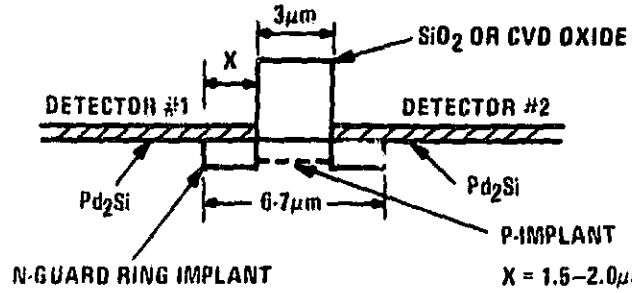


Fig. 4-9. Construction and operation of the vidicon readout.

There have been four detector isolation techniques studied in the process of designing the dual-band sensor. The four techniques are: (1) field oxide isolation, (2) poly field shield isolation, (3) continuous N guard ring isolation, and (4) modified field oxide guard ring isolation. The structure of each is detailed in Fig. 4-10.

The field oxide isolation technique was employed on the first design of the TA11395 high-density test chip. This technique depends upon the threshold of the boron doped region between the detectors to ensure isolation and absence of cross talk. The results of the first attempt with this technique were discouraging. The isolation was not adequate for the first TA11395 samples. However, there was a field threshold problem with these devices which was most probably the cause of the poor isolation. The conclusions to be drawn here are that the effectiveness of this technique is undesirably sensitive to process variations.

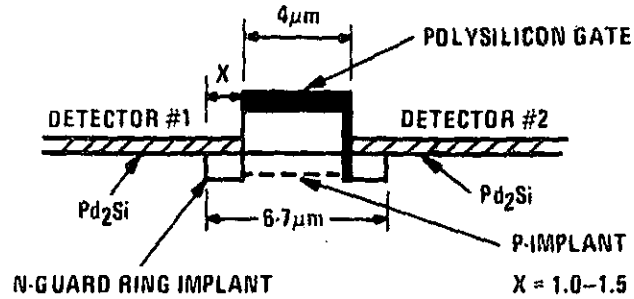
The poly field shield isolation technique employs a polysilicon gate between the detectors to deplete and isolate the region between the active detector areas. The polysilicon gate is biased with a negative potential to assure no charge transport between the detectors. This technique has been demonstrated to be effective on an RCA 64-x-128 Schottky barrier IRCCD. The design rules utilized for the 6-x-128 device were a mask defined polysilicon gate and a mask defined 7-μm polysilicon gate and a mask defined 4-μm N guard ring. This results in a mask defined 15-μm inactive region between detectors, and an after process dimension of 15.5 μm. These design rules would result in a fill-factor of 48% for a 30-μm SWIR detector.



MAXIMUM FILL-FACTOR = 80%

TA11395 ARRAYS CURRENTLY UNDER TEST

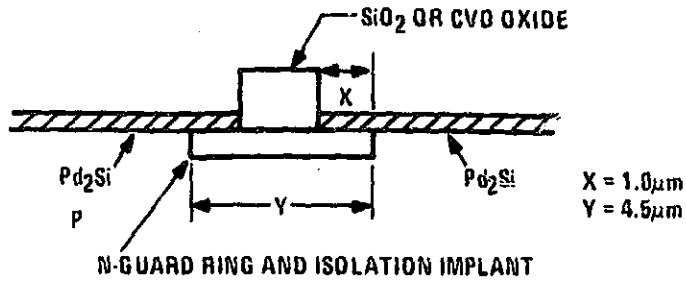
TECHNIQUE 1 – FIELD OXIDE ISOLATION



MAXIMUM FILL-FACTOR = 80%

TEST LINEAR ARRAYS TO BE PROCESSED ON 160 x 244 AREA ARRAY WAFERS

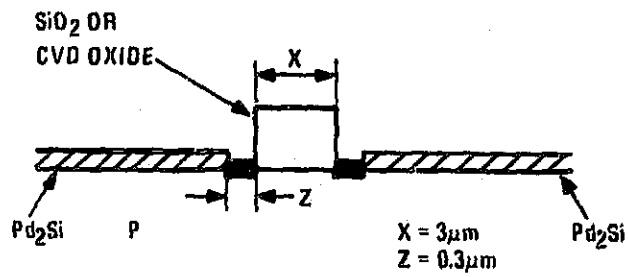
TECHNIQUE 2 – POLY FIELD SHIELD



MAXIMUM FILL-FACTOR = 87%

TC1247 AREA ARRAYS CURRENTLY UNDER TEST

TECHNIQUE 3 – CONTINUOUS N GUARD RING



MAXIMUM FILL-FACTOR = 88%

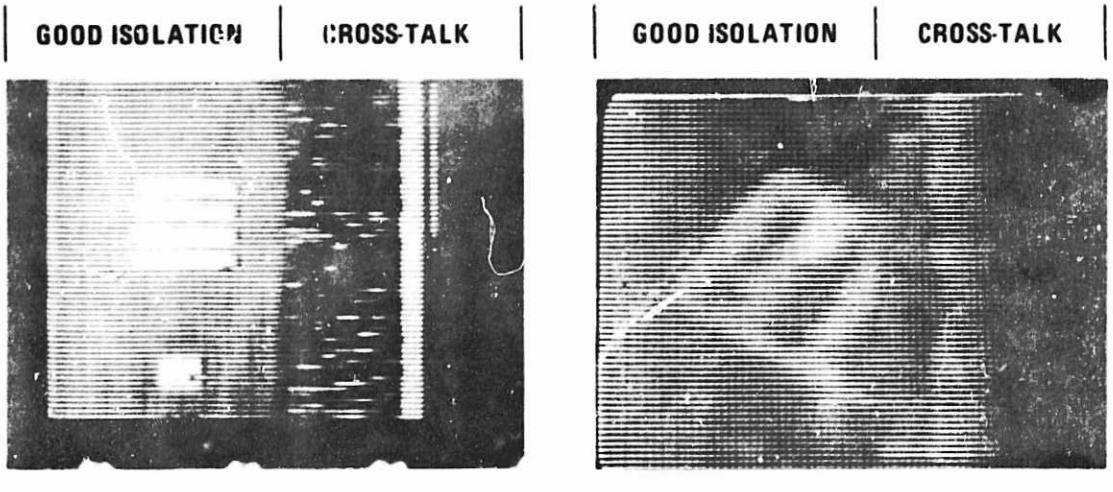
MASK OPTION FOR DUAL BAND SENSOR

TECHNIQUE 4 – MODIFIED FIELD OXIDE GUARD RING

Fig. 4-10. Detector isolation structures.

It is felt that the prudent approach to take on the first wafer lot of devices is to utilize the proven design rule, polysilicon isolation technique for 25% of the dual-band devices. A second 25% of the first wafer lot devices will utilize 4- to 5-μm polysilicon gates and 1.5- to 2-μm N guard rings. This will result in a mask defined 7- to 9-μm inactive region, and an after process dimension of 7.5 μm to 9.5 μm. The fill-factor for this design is thus 75% to 68%. The final decision on the precise dimensions will be made after examination of the geometric fidelity of the new version of the TA11395. The new high-density linear array has a 75% fill-factor, polysilicon isolation detector design. (Note: The SWIR schedule does not permit time to thoroughly test the 75% fill-factor design for dark current, noise, and cross-talk before committing to wafer fabrication of the dual-band sensor.)

The third approach to detector isolation is the continuous N guard ring technique. The technique forms back-to-back diodes to ensure isolation between detectors. The technique has been demonstrated on a Pd_2Si 32-x-64 area array (TC1247). Figure 4-11 shows test imagery produced by a TC1247 running in the vidicon mode. The left portion of the imager has a "properly designed" guard ring, the right portion exhibits the cross-talk produced when the geometric design is incorrect. This imager has an isolation structure which extends 19 μm. Measurements on test structures have shown that the region can be reduced substantially.



Pd_2Si TC1247 DEVICES, ISOLATION REGION OF 19μm

Fig. 4-11. Imagery produced by devices with N guard ring isolation.

This technique will be utilized for the remainder of the first wafer lot. There will be a 67% fill-factor design (mask defined 9 μm, after process 10-μm guard ring) and an 83% fill-factor design (mask defined 4 μm, after process 5-μm guard ring). These designs will be split equally to share 25% each of the first wafer lot.

The fourth isolation technique demonstrates the highest fill-factor option. This technique employs field oxide isolation, and a self-aligned guard ring. This structure does not have an isolation junction or channel stop. This option may have higher crosstalk levels than the other options, although this is not clear at present. The structure will have to be tested experimentally. The fill-factor is (27-x-30 μm)/(30-x-30 μm) = 90%. It should be noted that it may be possible to eliminate the guard ring structure completely if the detector dark current yield is low enough without guard rings.

Initial fabrication and experimentation that we conducted show that the breakdown voltage was over 35 V with and without self-aligned guard rings. This is an encouraging first look at the technique. This fourth isolation technique will be a mask option to be investigated on the second wafer lot of devices.

In summary, the first wafer lot will be divided into two generic detector isolation types. The first being the proven, fully characterized polysilicon isolation type. The second being the promising, partially characterized continuous N guard ring isolation type. Within each of these generic types, the first lot of parts will be divided between conservative and aggressive designs. The fill-factors associated with the four variations are given in Table 4-3. Measurement data from the first wafer lot will be utilized to choose one, or possibly two, approaches for the second wafer lot.

TABLE 4-3. DETECTOR FILL-FACTOR

Design Approach	Detector Size (μm)	Fill-Factor (%)
Conservative Polysilicon Isolation	30x14.5	48
Aggressive Polysilicon Isolation	30x20.5-22.5	68-75
Conservative Continuous N Guard Ring	30x20	68
Aggressive Continuous N Guard Ring	30x25	83

4.3 CCD REGISTER DESIGN

The CCD registers for the dual-band sensor will utilize the register design proven on the TA11395. The multiplexer registers will be buried n-channel CCDs with double polysilicon gates. A cross-section of the gate structure may be seen in Fig. 4-12. Each CCD will have a 30-μm pitch, with two second-level polysilicon and two first-level polysilicon gates per stage. The register will be suitable for both two-phase and four-phase clocking.

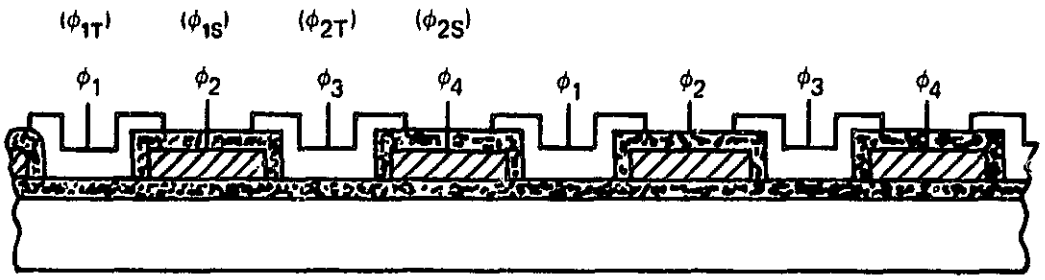
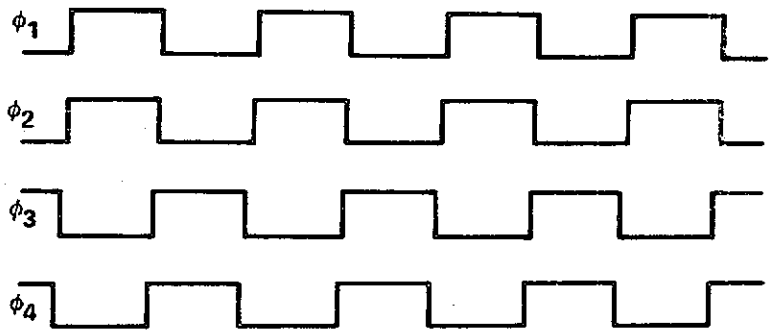


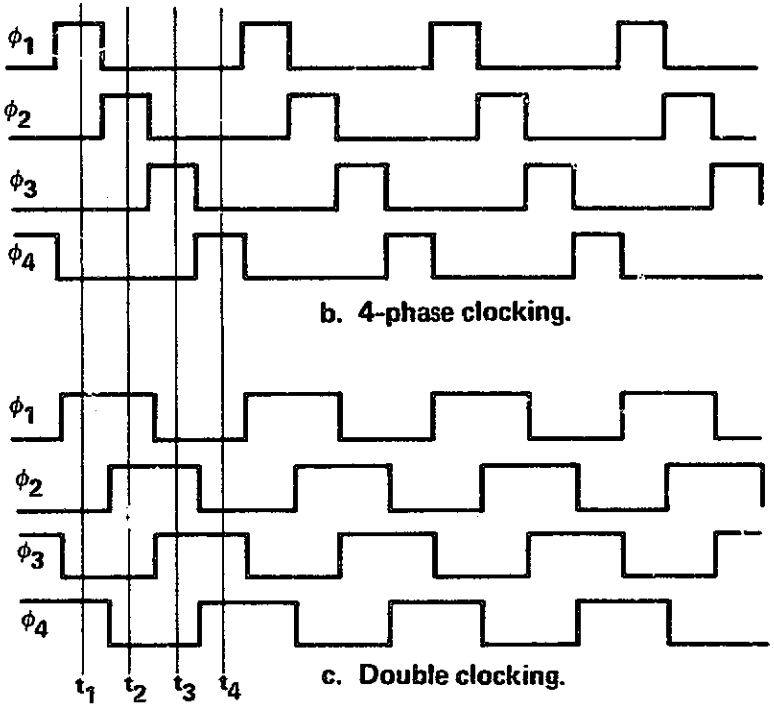
Fig. 4-12. Cross-sectional view of CCD.

The potential profiles representing two-phase clocking are shown in Fig. 4-13a. The potential profiles representing "normal" four-phase clocking are shown in Fig. 4-13b. The potential profiles of double-clocking four phase are shown in Fig. 4-13c. The length of potential wells with normal clocking and the length of potential wells with double clocking are illustrated in Fig. 4-13d and Fig. 4-13e, respectively. Since the four-phase, double-clocking mode stores charge under two electrodes, its signal-handling capacity is greater than that achieved with two-phase clocking. For a storage gate length of 10 μm and an exposed transfer gate length of 5 μm, the double-clocking, four-phase offers an increase in charge capacity of approximately 100% when compared with two-phase clocking. A summary of the clock tradeoffs is given in Table 4-4. With four-phase clocking there is the possibility of improved transfer efficiency per stage.

Our recommendation is to baseline the proven TA11395 register design, with the plans to utilize two-phase clocking. However, we will build a four-phase double-clocking capability into out next-generation electronics. Both clocking modes will be evaluated for transfer efficiency, register noise, feed-through characteristics, and charge capacity. If it is deemed advantageous, with a single mask option the CCD charge capacity may be tailored to the optimum width for the four-phase clocking mode. This is done by adjusting the channel stop mask to reduce the active channel width.

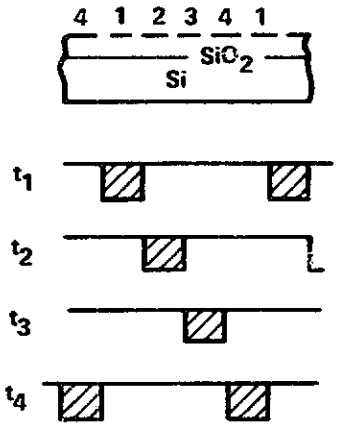


a. 2-phase clocking.

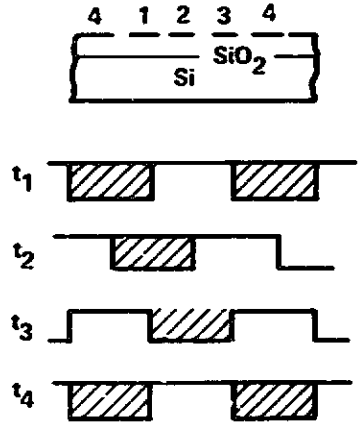


b. 4-phase clocking.

c. Double clocking.



d. Potential wells with normal clocking.



e. Potential wells with double clocking.

Fig. 4-13. CCD clocking options.

TABLE 4-4. CLOCK TRADEOFFS

	Two-Phase Double Clocking	Four-Phase Double Clocking
Number of Timing Waveforms	2	4
Signal Handling Capacity	Q_{max}	$2Q_{max}$+
Transfer Per Stage	2	4
Transfer Inefficiency Per Stage	$3x10^{-5}$*	To be measured

*TA11395, Room Temperature, 10% Fat Zero
+Dependent upon transfer gate dimension, this is the value for the most restricted region of the center tap serial register.

The CCD channel width must be chosen to assure nonblooming operation at the maximum signal level. The maximum signal in each band may be calculated with the following equation:

$$Q_{max} = \left[\frac{W_{max} A \tau Q_E \lambda}{hc}\right] \left[1 + \beta\right] \qquad (4\text{-}2)$$

where

W_{max} = maximum irradiance (W/cm^2)

A = detector active area (cm^2)

τ = integration time (s)

Q_E = quantum efficiency (decimal percent)

λ = wavelength (μm)

$h = 6.626x10^{-34}$ Joule-s

$c = 3x10^{14}$ $\mu m/s$

β = percent fat zero (decimal percent)

Table 4-5 gives the maximum signal level (in electrons) for each of the three bands of interest. We define the maximum signal level as the output produced by twice the maximum full-scale irradiance (MFSI) at the 4.4-ms integration time (Note: The RFP definition is 2xMFSI at 1.8 ms). The detector area is assumed to be 30 μm by 24 μm. The quantum efficiencies are assumed to be 20% at 1.25 μm, 14% at 1.65 μm, and 5.5% at 2.22 μm. The variable is the percentage of full well capacity to be used for fat zero bias charge. A recommendation of 10% bias charge is employed for the 2.22 μm band calculation of required capability. The calculations of capacity for the 1.25 μm and 1.65 μm band at the 4.4-ms integration time include no fat zero (in these large signal cases no bias charge should be required). Table 4-5 also gives the number of electrons constituting the signal at the working level irradiance (WLI) for the 1.8-ms integration time.

TABLE 4-5. BIAS CHARGE AND WLI SIGNAL

Wavelength (μm)	Signal at WLI (τ = 1.8 ms)	Twice MFSI ($\mu W/cm^2$)	Maximum Signal (τ = 4.4 ms)	Required Capacity
1.25	146,500	28.0	1,115,600	1,115,600
1.65	108,400	22.4	824,700	824,700
2.22	27,900	12.6	245,200	272,000

The CCD serial registers are sized to accommodate the maximum signal charge produced by the 1.25 μm band. As the table states this requirement is 1.1×10^6 electrons. The physical size of the CCD register was determined based on evaluation of the TA11395 charge capacity. The evaluation of the TA11395 has shown that with two phase clocking and 9-V clocks the charge capacity is 770,000 electrons for a storage gate area of 320 μm^2 (10x32 μm). This per unit area capacity was utilized to calculate the four phase and two phase charge capacity of the serial register with center tap (the details of transfer gate area were included). The design capacities are detailed in Table 4-6. The design will meet the NASA specified requirements.

TABLE 4-6. CCD REGISTER CAPACITY

Section	Area	Two Phase Capacity	Four Phase Capacity
Electrical Input (ac)	300 μm^2	720,000	720,000
Electrical Input (dc)	60 μm^2	114,000	114,000
Serial Register (fan)	237 μm^2	569,000	1,415,000
Serial Register (Standard)	250 μm^2	600,000	1,470,000
Left Center Tap	230 μm^2	553,000	1,161,000
Right Center Tap	240 μm^2	576,000	1,260,000
Usable Capacity	230 μm^2	553,000	1,161,000

4.4 CCD INPUT STRUCTURE

The serial CCD registers of the dual-band sensor will have electrical input stages. An electrical input is utilized for two functions. The first function of an electrical input is to provide bias charge (fat zero) to the CCD to improve transfer efficiency (if required). The second function of the input is to provide an accurate means of monitoring CCD register characteristics. It is the electrical input that is employed during register setup to optimize transfer efficiency.

The module will utilize the fill-and-spill electrical input technique. This input technique has proven to be a low-noise method for precise introduction of charge to CCDs. The structure is shown in Fig. 4-14. The bias charge is adjusted by the voltage differential between gates G1 and G2. The stage is operated by initially setting the diode voltage so that there is no charge introduction into the channel. The input diode is then pulsed so that a full well of charge is introduced into the G2 well (fill). The diode voltage is then restored to its initial level and the capacitance associated with the receiving well (G2) then discharges to a voltage level set by the voltage level on G1 (spill). The amount of charge introduced is equal to

$$Q_{BIAS} \approx 0.85\ (V_{G2}-V_{G1})\ C_{WELL} \qquad (4\text{-}3)$$

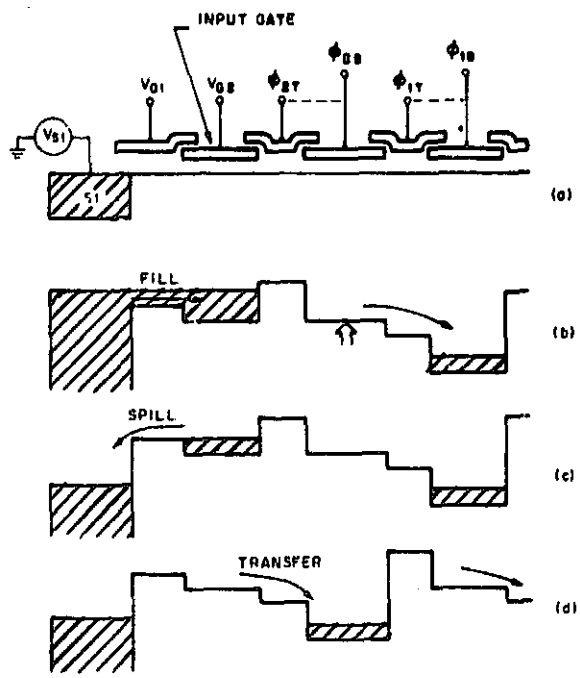


Fig. 4-14. Fill-and-spill input.

where

$$C_{WELL}(N_{SIG}) = \frac{1}{q\beta} \frac{\partial Q}{\partial V_{Gate}}$$

$$V_{MB} = \beta V_{GATE} \rightarrow \beta = 0.85$$

Proper design of the input to attain the correct value of capacitance (C_{WELL}) is important because it determines the charge capacity of the input stage as well as the noise introduced by the input. The noise introduced is a KTC noise which may be shown to be equal to

$$N_{rms} = \frac{1}{q} (KTC_{WELL})^{\frac{1}{2}} \qquad (4\text{-}4)$$

where

$T = 120K$

$K = 1.38 \times 10^{-23}$

$q = 1.6 \times 10^{-19}$ coulombs

Thus, C_{WELL} should be made small to minimize the noise contribution of the input; however, this compromises the charge injection capacity. To optimize the input performance further details of buried-channel devices operation need to be recognized.

It has been shown that for a buried-channel input the input capacitance (C_{WELL}) decreases as the signal size decreases. There are two effects which cause this decrease. First, the distance from the gate to the signal packet increases with decreasing signal, thus decreasing the capacitance. The second effect which decreases the effective capacitance for small signals is that the area occupied by the signal charge decreases. This is because for small values of signal charge, the signal packet contracts toward the potential minimum, which lies at the center of the gate. Results reported by Texas Instruments indicate that the effective capacitance at a 10% full well signal is approximately a factor of three less than that corresponding to 100% full well signal. Texas Instruments demonstrated that indeed a noise reduction of a factor of 1.7 is attained by running an input stage at 10% well capacity.

With this in mind, projections of noise performance may be completed. The maximum required charge capacity for the register is 1.1×10^6 electrons (0.20 pC). This can be realized with a $(V_{G2}-V_{G1}) = 2.75$ V and a $C_{WELL} = 0.85$. Extrapolation from measurements taken on the TA11395 predicts that a well capacitance of this size may be achieved with a G2 active gate area of approximately 512 μm^2. This design would give register electrical input noise of 74 rms electrons at high charge levels (> 75% full well) and a projected noise of 74/(1.7) = 43 rms electrons at 10% bias charge level.

These noise projections assume that there is no other noise mechanism at the input other than the KTC thermal noise. Consider, however, if there is 0.5 mV of fluctuation noise (i.e., pickup, feedthrough) between the voltage on the G1 gate and the voltage on the G2 gate. This would cause an additional noise contribution of (0.5×10^{-3} V/2.75 V) (2.7×10^5 electrons) = 49 rms electrons for the 2.22-μm band. This is greater than the KTC noise. Therefore, it is obvious that care must be taken to minimize coupling onto these control lines and these lines must be driven by low noise sources. The best way to affect these conditions is to bypass both the G1 and G2 lines as close as possible to the module. On the test assembly this would be done within 20 mils of the module. For individual module operation, this would be done as close as possible to the module evaluation socket. The problem with this approach is that the electrical input would not be able to accept an AC input for setup purposes.

The proposed solution is to have two electrical inputs per band. The first input will be used for setup, accommodating 1.5 times the register capacity. This register input will have G2 bypassed but will not have bypassing for G1. This will allow full exercise of the CCD register dynamic range with an AC input. The second input will be tailored for low noise bias charge introduction. The G1 and G2 lines for this input will be bypassed. As a further refinement of the CCD register tailoring technique, the input well capacitance for these input stages will be set for a maximum of 30% full well capacity. They will thus accommodate bias charge introduction of up to 30% full well. With this design, the KTC noise for an electrical bias charge of 10% will approach the values shown in Table 4-7.

TABLE 4-7. BIAS CHARGE INPUT NOISE (RMS ELECTRONS)

Tailored for 100% Full Well	74-43
Tailored for 30% Full Well	41-24

The implementation of this dual-input design is shown in Fig. 4-15. To run the setup input, S1, G1A, and G2 would be biased correctly and G1B would be off. To run the low-noise input, S1, G1B, and G2 would be biased correctly and G1A would be off.

4.5 CCD OUTPUT DESIGN

The output of each center tap serial CCD register will consist of a floating diffusion structure and a FET amplifier. These components of the module have received close attention because they have such a strong influence on signal-to-noise, bandwidth, power consumption, and linearity.

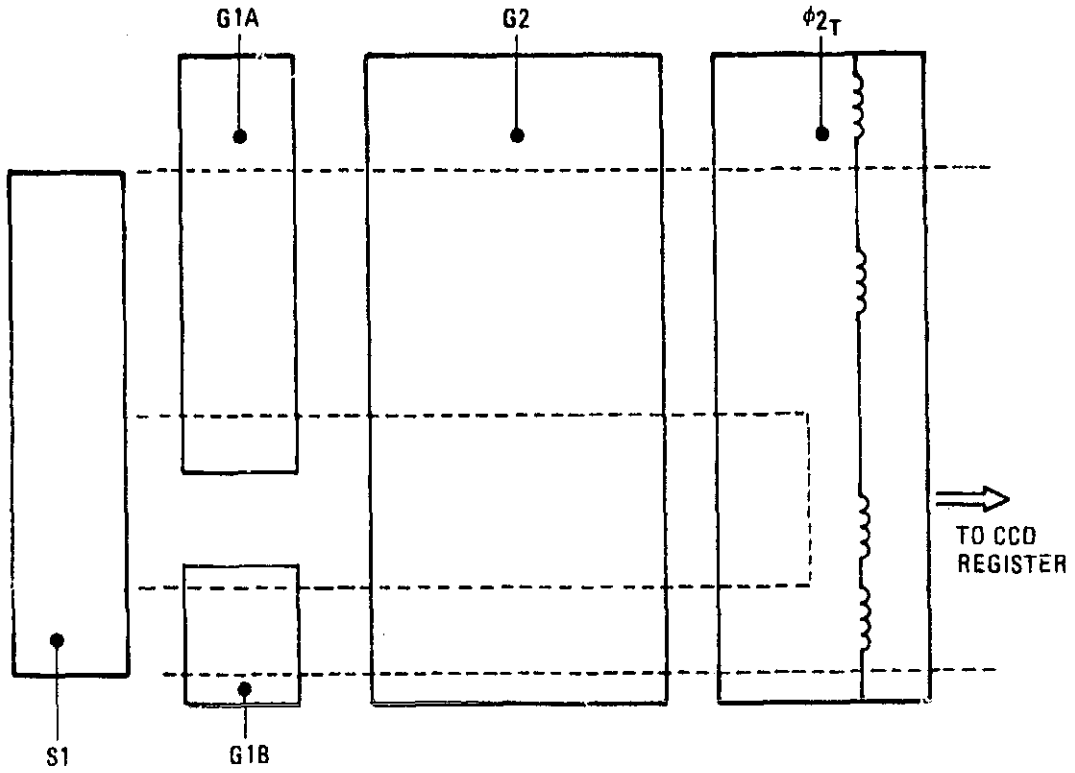


Fig. 4-15. Implementation of dual-input design.

For this application, the floating diffusion output technique is the superior choice when compared to the floating gate technique, or the distributed floating gate technique. The single-stage, floating gate output suffers from a reduced charge-to-voltage transfer gain when compared to a floating diffusion output. The multiple-stage, distributed floating gate amplifier is unattractive when considering linearity, reliability, and layout constraints. An optimized floating diffusion output design will give the highest signal-to-noise performance, with high reliability, high linearity, and low power dissipation.

4.5.1 Floating Diffusion Output Configuration

The CCD floating diffusion gate structure is shown in Fig. 4-16. The floating diffusion will have two DC gates on the sending side to receive charge from the left 256 detectors and right 256 detectors via the respective serial registers. The floating diffusion will have a DC isolation gate (ϕ_{DC3}) and a reset gate (ϕ_{RG}) on the reset drain (V_{DR}) side. The DC isolation gate will reduce the reset feedthrough onto the floating diffusion. This will allow the video amplifiers in the CDS to run with greater gain without saturation. There is a small penalty of increased floating diffusion node capacitance due to the effective extension of the floating diffusion by the DC gate. The calculated increase in capacitance is a tolerable 8%. The expected floating diffusion node capacitance is detailed in Table 4-8. For comparison the table also details the floating diffusion capacitance on the process test vehicle – the

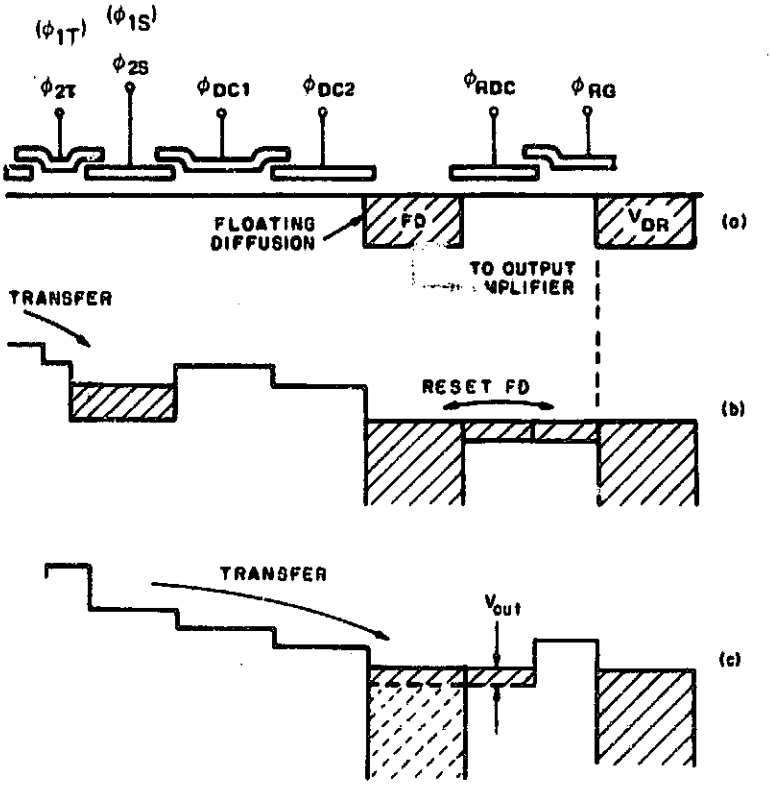


Fig. 4-16. Floating diffusion output.

TABLE 4-8. IMPROVEMENT IN FLOATING DIFFUSION NODE CAPACITANCE

$$V_{SIG} = Q_{SIG}/C_{FD}$$

$$C_{FD} = C_{FET} + C_{OXIDE} + C_{FIELD} + C_{DIODE} + C_{OVERLAP}$$

	Current Area Array	Proposed Array
C_{FET}	.037	.034
C_{OXIDE}	.060	.005
C_{FIELD}	.005	.005
C_{DIODE}	.018	.018
$C_{OVERLAP}$	.040	.019
$C_{TOTAL} = C_{FD}$	.16 pF	.08 pF
	• Non-self aligned (no field oxide)	• Self aligned (field isolated)

TC1247 (32-x-64 area array). As may be seen from the table, the dual-band module will have a voltage gain improvement of 0.16 pF/0.08 pF = 2 due to the reduction in capacitance. This capacitance reduction has the additional benefit of reducing the floating diffusion reset noise (KTC noise).

The center tap configuration utilizing one floating diffusion and one amplifier per 512 detector linear array will employ a "ping-pong" multiplexing. The common floating diffusion (FD) will alternately receive charge from the left and the right sides of the linear array, with a reset operation occurring between each charge sensing period. The operation of the multiplexer is portrayed in Fig. 4-17. There is a one-half stage of delay introduced into the right portion of the center tap serial register to achieve the "ping-pong," interlaced multiplexing (see Fig. 4-18).

The timing for the center tap operation is shown in Fig. 4-19. This diagram is drawn assuming two-phase clocking, four-phase clocking may also be accommodated. The diagram portrays the voltage output from the FD amplifier.

The single-stage, floating diffusion amplifier will be placed in close proximity to the output structure, with a minimum length of aluminum interconnect to the floating diffusion to maintain the low floating diffusion capacitance.

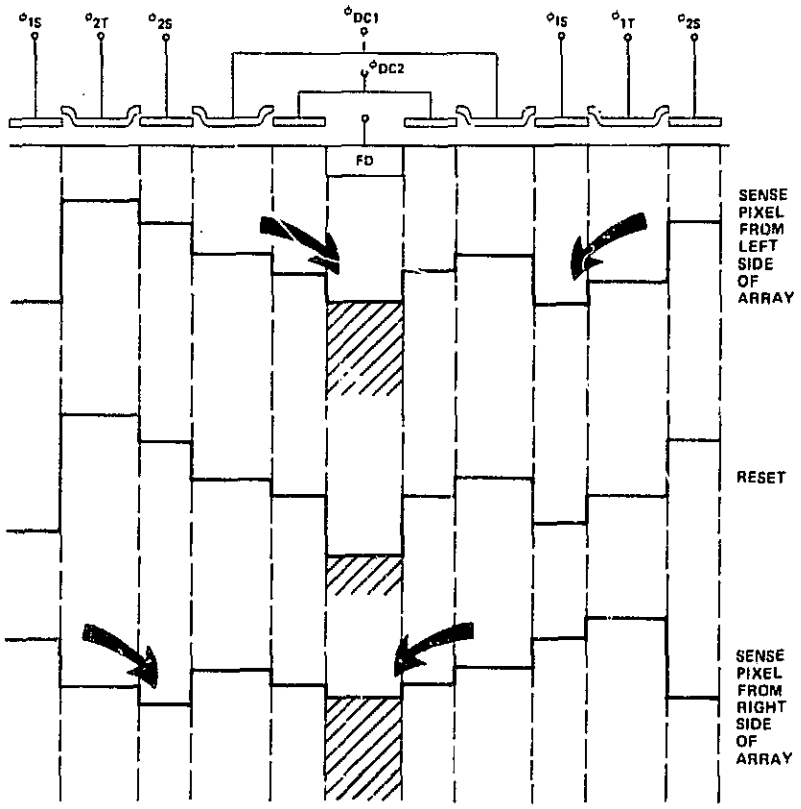


Fig. 4-17. Multiplexer operation.

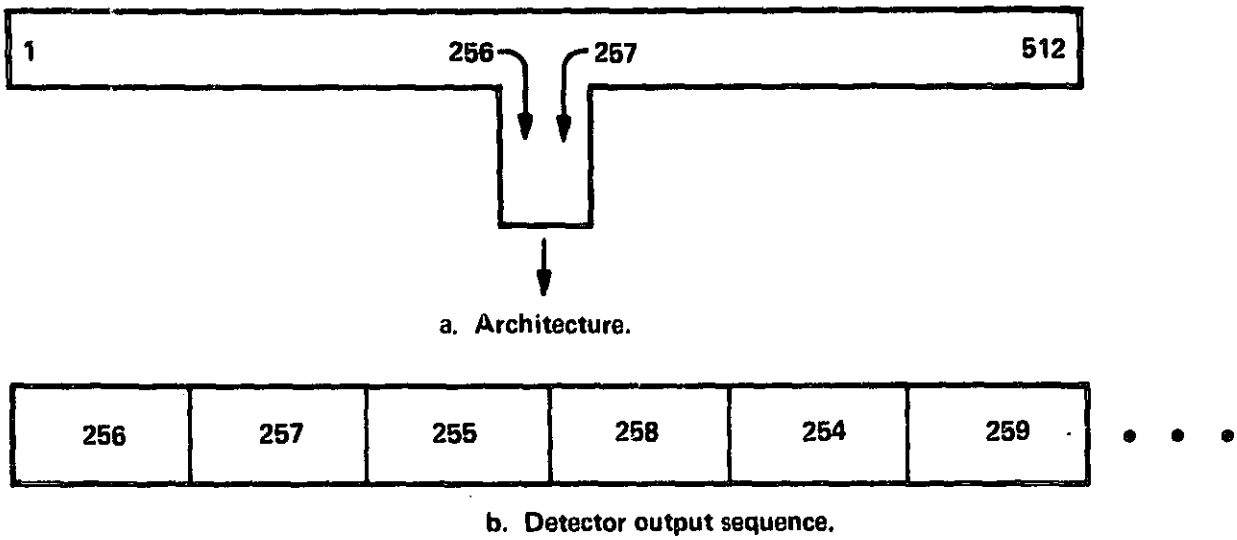


Fig. 4-18. Interlaced multiplexing.

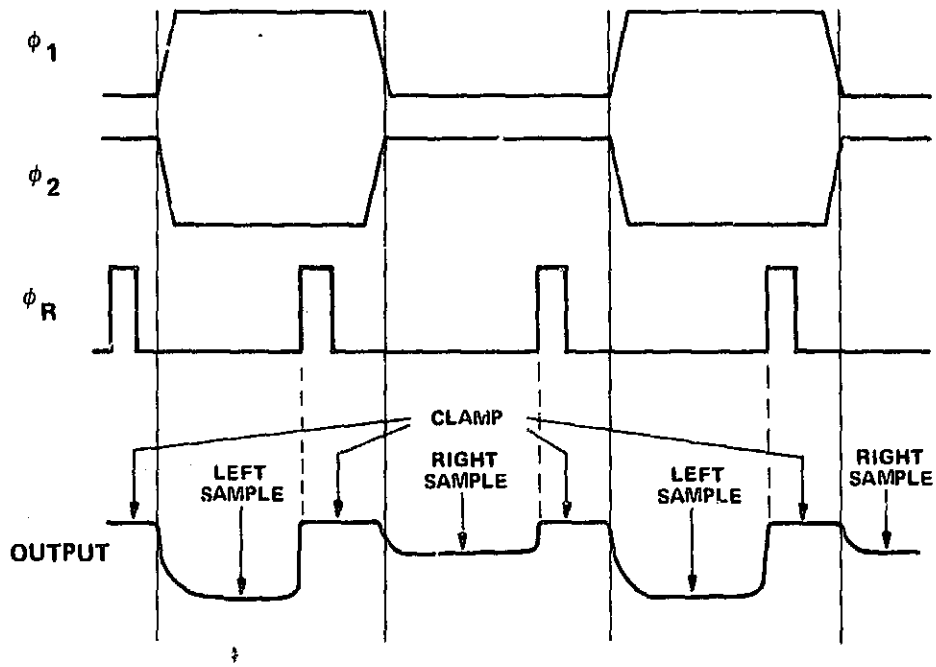


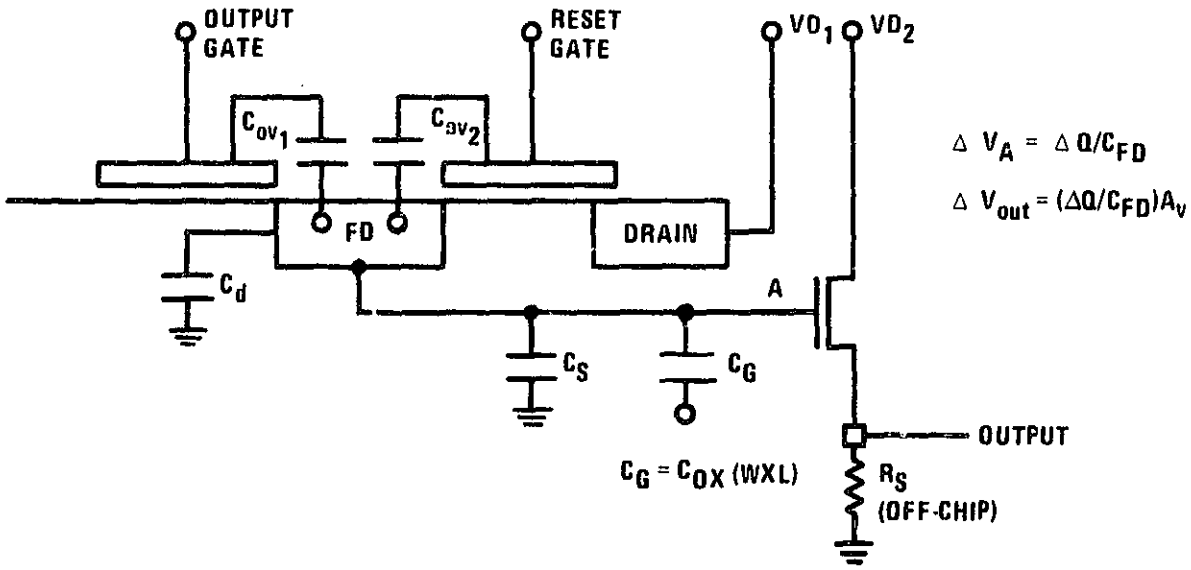
Fig. 4-19. Timing for center tap operation.

4.5.2 Minimizing Noise Contributed by the IRCCD Output Stage

To assure high signal-to-noise at the output of the dual-band SWIR arrays, particularly the 2.22-μm band which has the lowest projected quantum yield, it will be necessary to minimize noise contributed by the on-chip output stage. The output stage selected for the dual-band array is a floating diffusion amplifier containing a single on-chip FET. In this section it is shown that significant noise reduction can be achieved by: (1) using a buried-channel rather than a surface-channel FET to decrease FET 1/f noise; (2) optimizing the FET gate area to obtain the minimum combined KTC reset and FET 1/f noise; and (3) decreasing the floating diffusion depletion capacitance and the overlap and stray capacitance components to the minimum size possible.

4.5.2.1 Selected Floating Diffusion Amplifier Arrangement

The selected on-chip output stage, shown in Fig. 4-20, is a floating diffusion amplifier (FDA) containing an output gate(s), a floating diffusion, a reset gate, and a single buried-channel FET operated in the source follower mode (common drain configuration) with the source resistor, R_S, located off-chip. The output of the on-chip amplifier is fed into a low-noise J-FET buffer amplifier formed on a hybrid circuit and located close to the chip.



$$C_{FD} = C_d + C_{ov_1} + C_{ov_2} + C_S + C_G$$
$$= a + C_{ox}(WXL)$$

C_{ox} = 3.57 x 10^{-8} F/CM^2
W = FET GATE WIDTH
L = FET GATE LENGTH
a = 0.046pF, FOR TIGHT LAYOUT

Fig. 4-20. On-chip CCD floating diffusion output amplifier.

A buried-channel FET (BCFET) rather than a surface-channel FET (SCFET) is selected for the FDA because the BCFET results in significantly reduced 1/f noise. In a BCFET, the channel is physically removed from the trapping states at the silicon/silicon-dioxide interface which contribute to the high 1/f noise in SCFETs. The lower 1/f noise of BCFETs has been borne out by noise measurements made on the two types of devices both of which are contained on the TA11395 test IRCCD array.

By referring to Fig. 4-20 it is evident that the change in voltage resulting at node A from the change in charge transported by the CCD register is:

$$\Delta V_A = \frac{\Delta Q}{C_{FD}} \tag{4-5}$$

At the amplifier output the voltage change produced by ΔQ is

$$V_S = \Delta V_{out} = \frac{\Delta Q}{C_{FD}} A_v = \frac{\Delta N\ q\ A_V}{C_{FD}}$$

where

V_S = output signal voltage

ΔN = signal charge in electrons

q = electronic charge

A_v = voltage gain of the source follower

C_{FD} = capacitance associated with the floating diffusion

It is apparent that for a given signal charge, the signal voltage can be maximized by making C_{FD} as small as possible. C_{FD} consists of the parallel combination of the floating diffusion capacitance, C_d, the output gate-to-floating diffusion overlap capacitance C_{ov1}, the reset gate-to-floating diffusion overlap capacitance C_{ov2}, the stray or line capacitance C_s (which accounts for the aluminum and polysilicon trace-to-substrate capacitance, and the FET gate capacitance, C_G). Thus, the floating diffusion capacitance is

$$C_{FD} = C_d + C_{ov1} + C_{ov2} + C_s + C_G \tag{4-6}$$

representing $C_d + C_{ov1} + C_{ov2} + C_s$ with, a, and expressing

C_G as $C_G = C_{ox}$ (WxL) leads to

$$C_{FD} = a + C_{ox}\ (WXL) \tag{4-7}$$

where $C_{ox} = (\epsilon_{rox}\ \epsilon_o)/t_{ox}$

In equation W and L are the width and length of the FET gate, respectively, ϵ_{rox} is the relative dielectric constant of SiO_2, ϵ_o is the permitivity of the free space (8.85×10^{-14} F/cm^2), and t_{ox} is the oxide thickness. For an oxide thickness of 1,000 Å, the value used as the gate oxide thickness in our FETs,

$$C_{ox} = 3.57 \times 10^{-8}\ \text{F/cm}^2.$$

For a tight, integrated circuit layout utilizing present day design rules and processing technology, the floating diffusion capacitance parameter, a, can be made as small as 0.046 pF and a typical FET source follower gate area is 1.1×10^{-6} cm^2 (W = 10 μm, L = 11 μm) resulting in a typical value of C_{FD} of about 0.085 pF. This value of C_{FD} along with a typical value of A_V of 0.92 results in a signal output of about 1 μV per signal electron.

4.5.2.2 Noise Generated in the On-Chip Output Stage

Noise contributed by the on-chip FDA output stage consists of KTC reset noise, white thermal noise generated in the channel of the on-chip FET, and low-frequency FET flicker or 1/f noise. The FDA noise expressed in rms noise equivalent electrons is

$$\bar{N}_{KTC} = \left[\bar{N}^2_{KTC} + \bar{N}^2_{FET}\right]^{1/2} = \left[\bar{N}^2_{KTC} + \bar{N}^2_{1/f} + \bar{N}^2_{th}\right]^{1/2} \qquad (4\text{-}8)$$

where

$$\bar{N}_{KTC} = \frac{1}{q}\left[KTC_{FD}\right]^{1/2} \qquad (4\text{-}9)$$

and

$$\bar{N}_{th} = \frac{1}{q}\left[\frac{4KT\ \alpha\Delta f}{g_m}\right]^{1/2} C_{FD} \qquad (4\text{-}10)$$

In these equations,

K = Boltzman's constant (1.38×10^{-23} J/°K)

T = temperature in degrees kelvin

Δf = passband of interest

g_m = transconductance of the FET

α = coefficient whose value can range from 2/3 to 10

The quantity $[4KT\alpha\Delta f/g_m]^{1/2}$ is the full-band FET limiting thermal noise voltage referred to the input of the device. Our noise measurements on the BCFET of the TA11395 test IRCCD (when operated as a source follower with R_S = 10 kΩ and at the voltages applicable to CCD operation) have yielded 15.2 $nV/Hz^{1/2}$ as the room temperature limiting thermal noise voltage. The source follower voltage gain was measured to be 0.52 which results in an input referred thermal noise of 29.2 $nV/Hz^{1/2}$. From the measured value of g_m = 200 micromhos (at V_{DS} = 12 V and ΔV_G = 12 to 14 V) and for 1 MHz Δf, the approximate bandwidth to be used, the room temperature value of α is calculated to be close to 10. (It will be assumed that α will not change with temperature.)

The expression for the FET 1/f noise used here is

$$\bar{N}_{1/f} = \frac{1}{q} \frac{k\, C_{FD}}{(WxL)^{1/2}} \tag{4-11}$$

in which k is a measured FET 1/f noise coefficient applicable to a particular type of FET. The expression follows from the fact that the mean square FET 1/f noise voltage for a particular type of FET (buried or surface channel and having a given oxide thickness) is inversely proportional to FET gate area. That is,

$$\int_{f_1}^{f_c} (\bar{V}_{1/f}/Hz)\ df = \left[\frac{k^2}{(WxL)}\right]^{1/2} \tag{4-12}$$

where

f_1 = lower frequency of interest

f_c = 1/f noise corner frequency

The FET low-frequency noise of the BCFET on the TA11395 test IRCCD was measured. The noise voltage spectral density ($\bar{V}^2/Hz$ versus frequency) followed an $f^{-0.7}$ dependence with the corner frequency being close to 90 kHz. The integrated output noise over the frequency range 1 kHz to 90 kHz was 28 μV rms corresponding to an input referred low-frequency noise of 54 μV rms which for W = 11 μm and L = 10 μm yields k = 5.66×10^{-8} $V_{rms\text{-}cm}$ for the BCFET. Noise measurements were also made on the two-stage SCFET amplifier of the TA11395 test device. In this case, the input referred low-frequency FET noise attributed to the first stage amplifying FET (W = 6 μm and L = 14 μm) was determined to be 220 μV rms. Over the measured frequency range of 1 kHz to 1 MHz no corner frequency was found for the SCFET. From this data, the value of k applicable to the SCFET is 2.02×10^{-7} $V_{rms\text{-}cm}$.

4.5.2.3 FDA Noise for BCFET and SCFET of the TA11395 Test IRCCD

Before considering the optimization of the FET gate area to attain maximum signal-to-noise, it is of interest to examine the FDA noise which would result at the design temperature of 120K if the identical buried-channel FET floating

diffusion amplifier of the TA11395 test device were to be used in the dual-band array. The results, summarized in Table 4-9, show that KTC reset noise would be the dominant noise source. The corresponding FDA noise for a similar FDA, but using the noise characteristics measured for the SCFET, are shown in Table 4-9 in parentheses. Here, it is seen that because of its large 1/f noise the SCFET 1/f noise would be the dominant noise component and that SCFDA noise exceeds th of the BCFDA by a factor of about 1.6. The KTC reset noise of SCFDA is lower than that of the BCFDA because the SCFDA floating diffusion capacitance is less (0.077 pF versus 0.085 pF for the BCFDA).

TABLE 4-9. NOISE EXPECTED AT 120K FOR THE BURIED-CHANNEL FDA OF THE TA11395 TEST IRCCD ARRAY

Noise Source	Number of Noise Equivalent Electronics*	
KTC Reset	74	(70)**
FET Thermal	10	(0)
FET 1/f	29	(105)
$\bar{N}_{FDA}$	80 e^-	(126 e^-)

*BCFET, WxL=1.1x10^{-6} cm^2, T=120K, a=0.046 pF, C_G=0.034 pF, C_{FD}=0.08 pF, BW=1 MHz, k=5.66x10^{-8} V-cm, f_{crnr}=90 kHz, α = 10. Assumes no change in FET 1/f noise with temperature.

**Parentheses enclose corresponding values for SCFDA.

4.5.2.4 Obtaining the Minimum FDA Noise

The FDA noise of equation 4-8 may be expressed as

$$\bar{N}_{FDA} = \left[\frac{1}{q^2} KTC_{FD} + \frac{1}{q^2}\frac{k^2}{(WxL)} C_{FD}^2 + \frac{1}{q^2}\frac{4KT\alpha\Delta f}{g_m} C_{FD}^2\right]^{1/2} \quad (4\text{-}13)$$

or

$$\bar{N}_{FDA} = \left[\frac{1}{q^2} KT_{CFD}(a+C_{ox}(WxL)) + \frac{1}{q^2}\frac{k^2}{WxL}(a+C_{ox}(WxL))^2 + \frac{1}{q^2}\frac{4KT\alpha\Delta f}{g_m}(a+C_{ox}(WxL))^2\right]^{1/2} \quad (4\text{-}14)$$

Plots of the three noise components versus FET gate area are shown in Fig. 4-21 for an FDA output stage using a BCFET and operating at the design temperature of 120K. Because the FET thermal noise is seen to be small compared to the KTC reset noise, it will be neglected for the purpose of determining the FET gate area required for minimum noise or equivalently for maximum signal-to-noise. The combined reset and FET noise is

$$\left[\bar{N}^2_{KTC} + \bar{N}^2_{1/f}\right]^{1/2} = \frac{1}{q}\left[KT(a+C_{ox}(WxL)) + \frac{k^2}{(WxL)}\,(a+C_{ox}(WxL))^2\right]^{1/2} \qquad (4\text{-}15)$$

and has a minimum value when (WxL), the FET gate area, is

$$(WxL) = \frac{ka}{\left[KTC_{ox} + k^2\ C_{ox}{}^2\right]^{1/2}}\ , \text{(for minimum noise)} \qquad (4\text{-}16)$$

and the value of C_{FD} at minimum noise is therefore

$$C_{FD} = a + \frac{a\ C_{ox}\ k}{[KTC_{ox} + k^2\ C_{ox}{}^2]^{1/2}}\ , \text{(at minimum noise)} \qquad (4\text{-}16a)$$

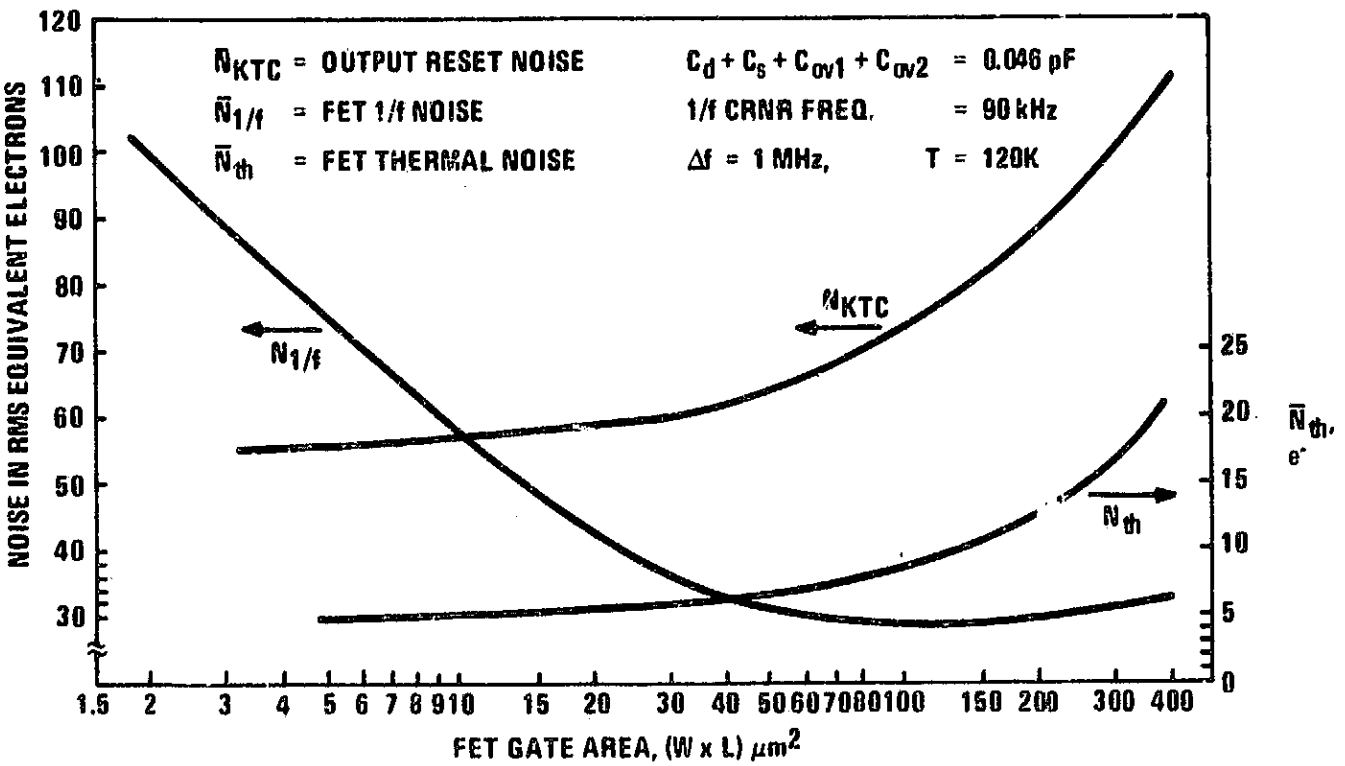


Fig. 4-21. Noise components of output BCFET floating diffusion amplifier vs. FET gate area.

Using the parameters applicable to the FDA having a BCFET, the FET gate area required for minimum noise is 33 μm^2 and the total noise (to which a thermal noise of $6e^-$ has been added is 71 noise electrons. The results are summarized in Table 4-10. A comparison with Table 4-9 shows that for the optimized case the KTC noise has been decreased, while the FET 1/f noise has been increased. It is also evident that optimizing the FET gate area results in only nine fewer noise electrons than would be attained using the non-optimized FET gate area (110 μm^2) of the TA11395 BCFET.

TABLE 4-10. MINIMUM NOISE EXPECTED AT 120K FOR AN FDA CONTAINING A BCFET

Noise Source	Number of Noise Equivalent Electrons*	
KTC Reset	61	(71)**
FET Thermal	6	(0)
FET 1/f	35	(120)
N_{FDA}	71 e^-	(124 e^-)

*BCFET, WxL=$3.3x10^{-7}$ cm^2, T=120K, a=0.046 pF, C_G=0.012 pF, C_{FD}=0.058 pF, BW=1 MHz, k=$5.66x10^{-8}$ V-cm, f_{crnr}=90 kHz, α = 10.
**Parentheses enclose minimum noise values for SCFET, WxL=$8.8x10^{-7}$ cm^2, a=0.046 pF, C_G =.031 pF, C_{FD}=0.077 pF, BW=1 MHz, k=$2.02x10^{-7}$ V-cm.

For the higher 1/f noise SCFET, whose values are enclosed in parentheses in Tables 4-9 and 4-10, the decrease in FDA noise is even smaller (only 2 noise electrons). It can be seen, however, that the optimized BCFDA is significantly less noisy than the optimized SCFDA ($71e^-$ versus $124e^-$).

From this, it is evident that the FDA of the dual-band array should contain a BCFET and that further decrease in the FDA noise will require reducing the floating diffusion capacitance parameter, a, to less than the presently attainable value of 0.046 pF.

Plots of the FDA noise versus FET gate area are given in Fig. 4-22 and 4-23 for the BCFDA and SCFDA, respectively. In both cases it is seen that the minimum is rather broad and that the rate of increase of noise as the FET gate area is increased relative to the optimum gate area is small. For example, a two-fold increase in the optimum gate area of the BCFDA (from 33 to 66 μm^2) results in only three additional noise electrons.

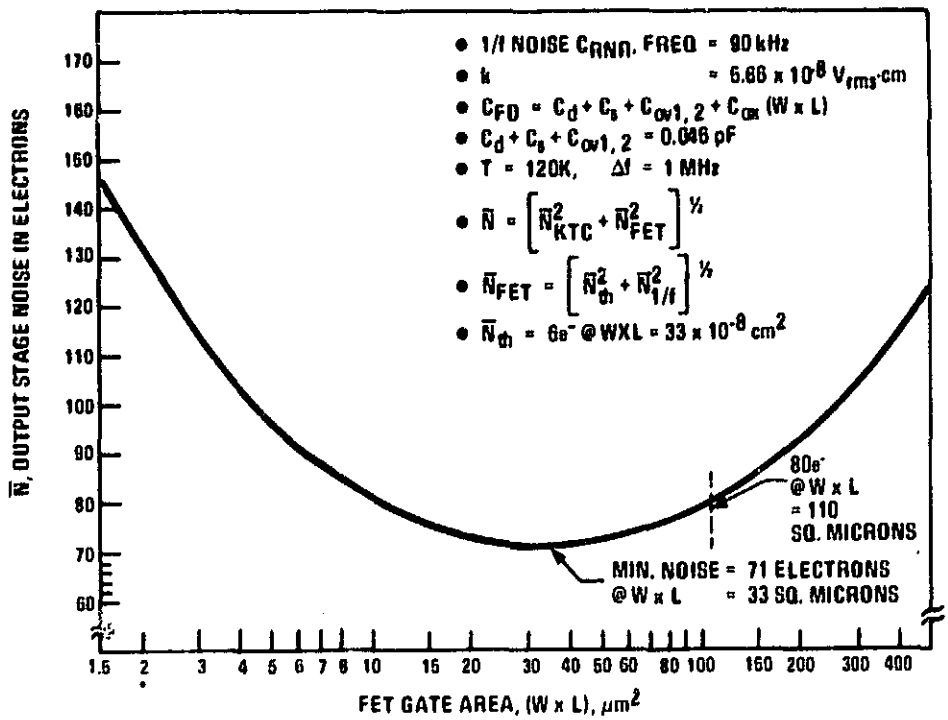


Fig. 4-22. Buried-channel FET combined reset and FET noise vs. FET gate area.

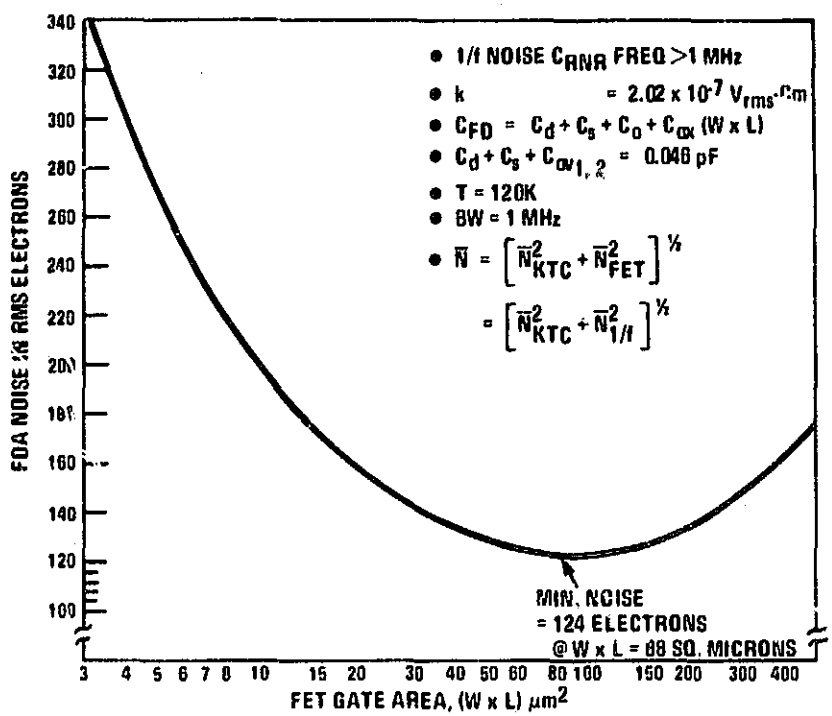


Fig. 4-23. Surface-channel FET combined reset and FET noise vs. FET gate area.

4.5.2.5 Dependence of Minimum Attainable FDA Noise on the Floating Diffusion Capacitance Parameters

The dependence of the minimum attainable combined KTC reset and FET 1/f noise for an FDA using a single FET on the floating diffusion capacitance parameter, a, is given by

$$[\bar{N}_{KTC} + \bar{N}^2_{1/f}]_{min} = \frac{1}{q}\, a[KT+2K^2C_{ox}] + 2ka\,[KTC_{ox}+k^2C_{ox}^2]^{1/2}\,^{1/2} \qquad (4\text{-}17)$$

A plot of this function is shown in Fig. 4-24 which also shows the optimum FET gate area as a function of the floating diffusion parameter, a. The curves apply to a BCFET of the type used in the TA11395 test IRCCD.

It is evident that the IRCCD design and layout (and processing) should be carefully selected to minimize a. If the current value of a = 0.046 pF can be reduced to 0.023 pF, the FDA noise will decrease to 51 noise electrons. On the other hand, if the layout were to lead to an increase in a to 0.092 pF, the FDA noise will increase to 100 noise electrons. Utilizing the current IRCCD process and the amplifier design to be described in the following section the value of a = .046 pF and the WxL product is 110 μm^2.

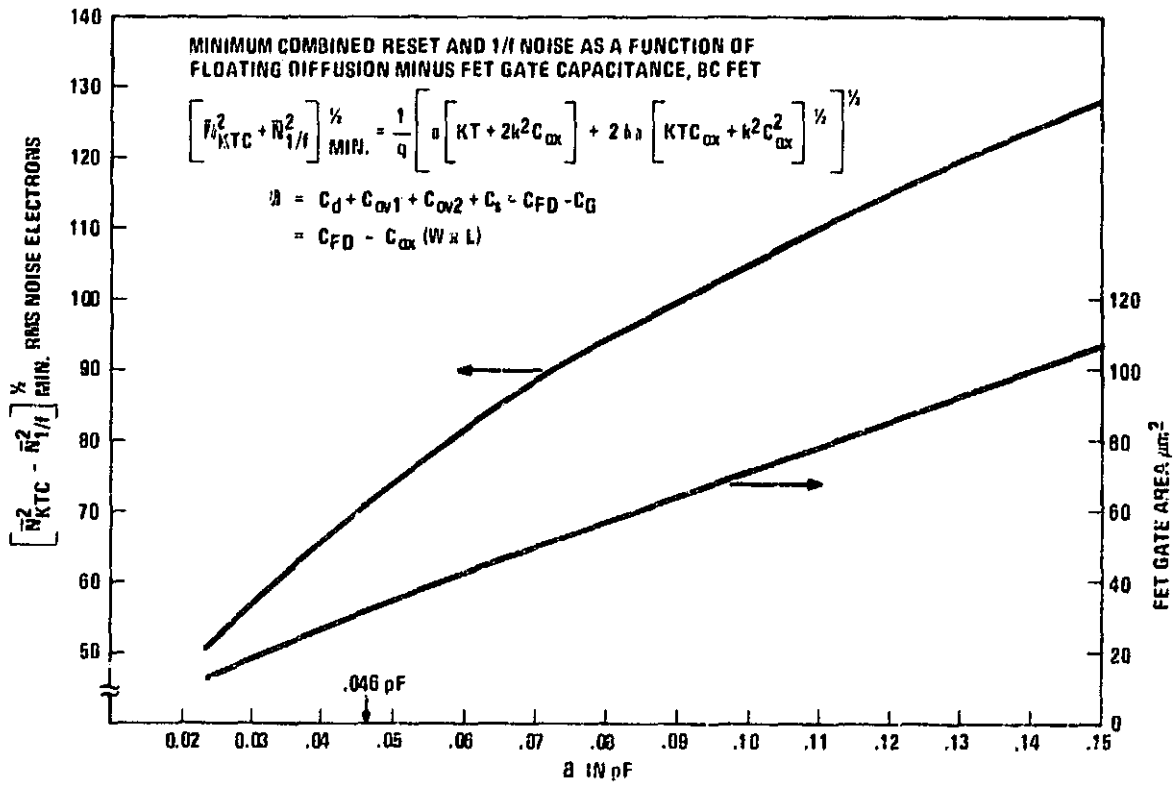


Fig. 4-24. Minimum combined reset and 1/f noise for BCFET.

4.5.2.6 Signal-to-Noise

Consideration is now given to the projected signal-to-noise in the 2.22-μm band for four cases in which the signal charge in each is 27,900 electrons corresponding to a detector area of 30 μm by 24 μm (80% fill factor), quantum yield of 5.5%, integration time of 1.8 ms, and working level irradiance of 3.5×10^{-6} W/cm^2. In each case the array is assumed to be maintained at a temperature of 120K. The four cases are:

- Case A - This is the proposal goal in which the CCD gates and fat zero electrical input structure were sized for a full-well charge of 1.51×10^6 electrons (the same size as for the 1.25- and 1.65-μm bands), but with the signal charge now reduced to the previously noted 27,900 electrons.
- Case B - Here the CCD gates and fat zero electrical input structure are sized for a smaller full-well charge (2.72×10^6 electrons) which is more appropriate for the signal in the 2.22-μm band. The signal in the 2.22-μm band will be appreciably less than in either the 1.25- or 1.65-μm bands (approximately 19% of the 1.25-μm band and about 26% of the 1.65-μm band signals) because of the lower quantum yield. Because the fat zero charge is 10% of the reduced full-well charge, transfer fluctuation loss and bulk state trapping noise, both of which are fat zero charge amplitude dependent, are reduced relative to Case A. Additionally, because the electrical input structures are now smaller, the KTC input noise will also be reduced. Case B further assumes an FDA having a SCFET but with the gate area sized for minimum SCFDA noise (124 electrons). No correlated double sampling circuit to further reduce the FDA noise is assumed. **(Note: Recently a technique has been devised which provides CCD capacity of over 10^6 electrons, yet permits fat zero bias charge to be reduced to levels comparable to those used in the calculation for N_{SAT}= 2.72×10^6 electrons. Thus, these calculations are indicative of expected performance).**
- Case C - This case is identical to Case B with the exception that a BCFET of gate area sized for minimum FDA noise is used resulting in a reduced FDA noise of 71 electrons.
- Case D - This is Case C but with the addition of a correlated double sampling circuit which is assumed to reduce the FDA noise of Case C by a factor of 2.5.

The results of the calculations for the four cases are shown in Table 4-11. The equations used to calculate the various noise components are given in Table 4-12 and the noise parameters of the buried- and surface-channel FETs used in the calculations, for Cases B, C, and D, are given in Tables 4-13 and 4-14.

As is seen from Table 4-11, the largest noise component (other than the essential background photon shot noise) is the transfer loss fluctuation noise for the cases C and D which employ a BCFET in the floating diffusion amplifier (75 electrons). The second largest noise term for cases C and D is the detector reset noise (60 electrons) which may possibly be reduced if the array can be operated in the continuous charge skimming mode rather than in the presently planned vidicon mode.

TABLE 4-11. PROJECTED SIGNAL-TO-NOISE FOR THE 2.2-μm BAND NOISE

NOISE COMPONENTS (T = 120K)	(A) • PROPOSAL GOAL[a] • CONVENTIONAL HIGH CAPACITY CCD • WITH CDS	(B) • WITH SCFET[b] • HIGH CAPACITY WITH LOW BIAS CCD • W/O CDS	(C) • WITH BCFET[c] • HIGH CAPACITY WITH LOW BIAS CCD • W/O CDS	(D) • WITH BCFET • HIGH CAPACITY WITH LOW BIAS CCD • WITH CDS[d]
• TRANSFER LOSS FLUCTUATION	135	75	75	75
• BULK STATE TRAPPING	68	41	41	41
• INPUT KTC NOISE	53	34	34	34
• DETECTOR RESET[e]	60	60	60	60
• DETECTOR DARK CURRENT	13	13	13	13
• CCD DARK CURRENT	5	5	5	5
• FDA NOISE, (KTC RESET), ($FET_{1/f}$), (FET_{th}).	100	124	71 (61), (35), (6)	28
• RMS SUB TOTAL	199	166	131	114
• PHOTON SHOT NOISE= $\sqrt{N_S}$ =$\sqrt{29,700}$	167	167	167	167
• RMS TOTAL, ($\bar{N}_T$)	260	236	212	202
• S/N = 27,900/$\bar{N}_T$	107	118	132	138
• % OF IDEAL S/N	64	71	79	83
• NOISE FLOOR ≈NOISE EQ. SIG.	191e^-	155e^-	117e^-	97e^-

(a) DETECTOR AREA 30μm x 24μm (ALL CASES)
(b) SCFET GATE AREA SIZED FOR MIN. FDA NOISE
(c) BCFET GATE AREA SIZED FOR MIN. FDA NOISE
(d) ASSUMES CDS REDUCES FDA KTC & FET 1/f NOISE BY FCTR. OF 2.5
(e) DETECTOR 1/f NOISE HAS NOT BEEN QUANTIFIED

TABLE 4-12. EQUATIONS USED IN NOISE CALCULATIONS OF TABLE 4-11

- TRNSFR LOSS FLUCT. (75e⁻) $\bar{N}_{xfer} = [2\epsilon N_g (N_s + N_{FZ})]^{1/2}$
- BULK ST. TRPNG (41e⁻) $\bar{N}_{BULK} = [0.5 \bar{N}_g \bar{N}_t V_g]^{1/2}$
- INPT. KTC (34e⁻) $\bar{N}_{in\ KTC} = \frac{1}{q}[KTC_{in}]^{1/2}$
- DET. RESET (60e⁻) $\bar{N}_{Det\ KTC} = \frac{1}{q}[KTC_{Det}]^{1/2}$
- DET. 1/f NOISE TO BE DETERMINED
- DET. DRK CURRENT SHOT (13e⁻) $\bar{N}_{Det\ DK} = \left[\frac{1}{q} J_{dK}\, t_{int}\, A_d\right]^{1/2}$
- CCD DRK. CURRENT SHOT (5e⁻) $\bar{N}_{CCD\ DK} = \left[\frac{1}{q} J_{dK_c}\, t_{int}\, A_s\right]^{1/2}$
- FD AMPLIFIER (71e⁻, BCFET) $\bar{N}_{FDA} = \left[\bar{N}^2_{KTC} + \bar{N}^2_{1/f} + \bar{N}^2_{th}\right]^{1/2}$
- BCKGND PHOTON SHOT, [27,900]$^{1/2}$ e⁻ $\bar{N}_s = \sqrt{N_s}$

(VALUES IN PARENTHESIS ARE FOR 2.22μm BAND OPERATING AT WLI, τ = 1.8 ms)

ϵ = 5×10^{-5}/xfer
N_g = (2) (512) xfers
N_s = 27,900e⁻
N_{FZ} = 27,000e⁻
N_t = 3×10^{11} cm^{-3}
V_g = (2×10^{-16}) (NEST + N_{FZ}) Cm^3
q = 1.6×10^{-19}C/e⁻
K = 1.38×10^{23} J/°K
T = 120K
C_{in} = 0.018 pF, = (6.9×10^{-20}) ($10N_{FZ}$)
C_{Det} = 0.056 pF
J_{dK} = 2 nA/cm^2
t_{int} = 1.8 ms
A_d = 30μm x 24μm
J_{dKC} = 0.2 nA/cm^2
A_s = 30μmx 18μm
λ = 2.22μm
Q_E = 5.5%

TABLE 4-13. BURIED-CHANNEL FET NOISE

$W = 11\mu m$ $L = 10\mu m$

$A_V = 0.52$ WITH $10K\Omega$ R_S, $g_m = 200\mu mhos$

- **LOW FREQUENCY NOISE**
- "1/f" CORNER FREQUENCY $\approx$ 90 kHz (SLOPE = -0.7)
- NOISE VOLTAGE (1 kHz TO 90 kHz) = $28\mu V$ (@ OUTPUT) = $54\mu V$ (@ INPUT)
- LOW FREQ NOISE IN RMS ELECTRONS = $29e^-$
- $k = (v_{1/f\ input})\ (W \times L)^{1/2} = 5.66 \times 10^{-8}$ V-cm

- **LIMITING THERMAL NOISE**
- $v_{th}/Hz^{1/2}$ = 15.2 nV/$Hz^{1/2}$ @ OUTPUT = 29.2 nV/$Hz^{1/2}$ @ INPUT
- v_{th} (90 kHz TO 1 MHz) = $28\mu V$ @ INPUT, (300K) = $18\mu V$ @ INPUT, (120K)
- N_{th} (90 kHz TO 1 MHz) = $15e^-$, (300K) = $10e^-$, (120K)

- **FULLBAND BC FET NOISE (1 kHz TO 1 MHz)**
- $\left[\bar{v}_{1/f}^2 + \bar{v}_{th}^2\right]^{1/2}$ = $61\mu V$, (300K) = $57\mu V$, (120K)
- $\left[\bar{N}_{1/f}^2 + \bar{N}_{th}^2\right]^{1/2}$ = $33e^-$, (300K) = $31e^-$, (120K)

TABLE 4-14. SURFACE CHANNEL FET NOISE

FIRST STAGE FET DIMENSIONS
W = 6 μm, L = 14μm
TOTAL GAIN A_V = 0.63, (A_{V_1} = 0.9, A_{V_2} = 0.7)

- **LOW FREQUENCY NOISE**
- **"1/f" CORNER FREQUENCY** $>$ **1 MHz**
- **NOISE VOLTAGE (1 kHz TO MHz)** = **154 μV @ OUTPUT**
  = **220 μV @ INPUT**
- **LOW FREQ NOISE IN ELECTRONS** = **105e$^-$**
- **k = (v_n 1/f INPUT) (W x L)$^{1/2}$** = **2.02 x 10^{-7} V-cm**
- **FULLBAND SC FET NOISE (1 kHz to 1 MHz)**

$\bar{v}_{1/f}$ (1 kHz TO 1 MHz) = 220 μV, (300K OR 120K)

$\bar{N}_{1/f}$ = 105e$^-$, (300K OR 120K)

FOR EQUAL GATE AREA $\dfrac{\bar{N}_{1/f}\ \text{SC FET}}{\left[\bar{N}_{1/f}^2 + \bar{N}_{th}^2\right]^{1/2}\ \text{BCFET}} = \dfrac{105e^-}{31e^-}\left[\dfrac{84\mu m^2}{110\mu m^2}\right]^{1/2} = 3$

OPTIMIZED BC FET AMP NOISE = $\frac{1}{3}$ OPTIMIZED SC FET AMP NOISE

Table 4-11 shows that the best chance of realizing the desired signal-to-noise ratio of 110:1 in the 2.2-μm band is afforded by Case D for which the projected signal-to-noise is 83% of the ideal signal-to-noise ($N_S^{1/2}$). The noise floor projected for Case D is 97 electrons which is essentially the noise equivalent signal for this case.

It should be noted that the noise components given in Table 4-11 do not include all of the noise terms that can be experienced in an actual CCD array. For example, pickup and clock noise, which cannot be calculated are not included. Also, noise contributed by the off-chip J-FET buffer amplifier, although expected to be small, has not been accounted for. Further, it is not certain that the CDS circuit will reduce the KTC reset and FET 1/f noise component by as much as the here-assumed factor of 2.5.

4.5.3 Design of Buried-Channel Amplifier

The design of the buried-channel amplifier was greatly simplified by using the RCA computer simulation program R-CAP. The process descriptive inputs to R-CAP were first adjusted to obtain results which matched measured laboratory data. Using this as a starting point, design parameters were then varied to obtain circuit characteristics which fell within design constraints.

The first step was to match DC characteristics. R-CAP was executed using a voltage ramp function as the source follower input. The output was then plotted versus this ramp input. The R-CAP parameters electron mobility (MN), threshold voltage (VTN), and conductance of saturation region (SLN) were varied until the relative magnitude and slope of the R-CAP plot matched that of the measured characteristic of the buried-channel source follower on the TA11395 (see Fig. 4-25).

Next, the AC characteristics were simulated using the results from the DC test. A 2-FET floating diffusion amplifier configuration (Fig. 4-26) was modeled using the previously DC-optimized FET as the follower. The R-CAP parameters were then varied so that the fall time and DC offset of the source follower output matched the measured laboratory data (TA11395) for similar AC input signals (see Fig. 4-27). A photograph of the TA11395 buried-channel floating diffusion amplifier output is shown in Fig. 4-28.

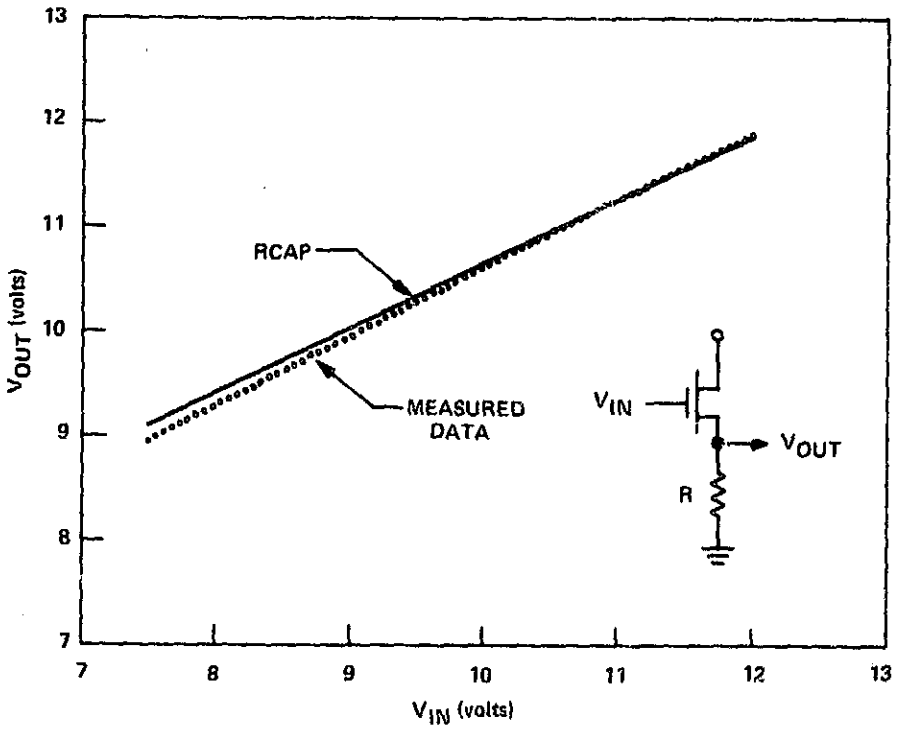


Fig. 4-25. FET amplifier R-CAP model with SLN=.04, MN=550, VTN=-8.5, and R_S=20K, C_S=20 pF.

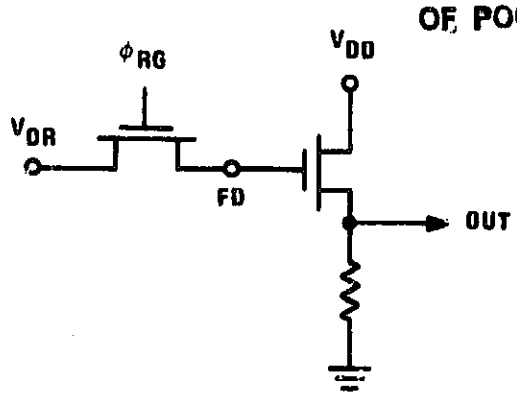


Fig. 4-26. 2-FET floating diffusion amplifier.

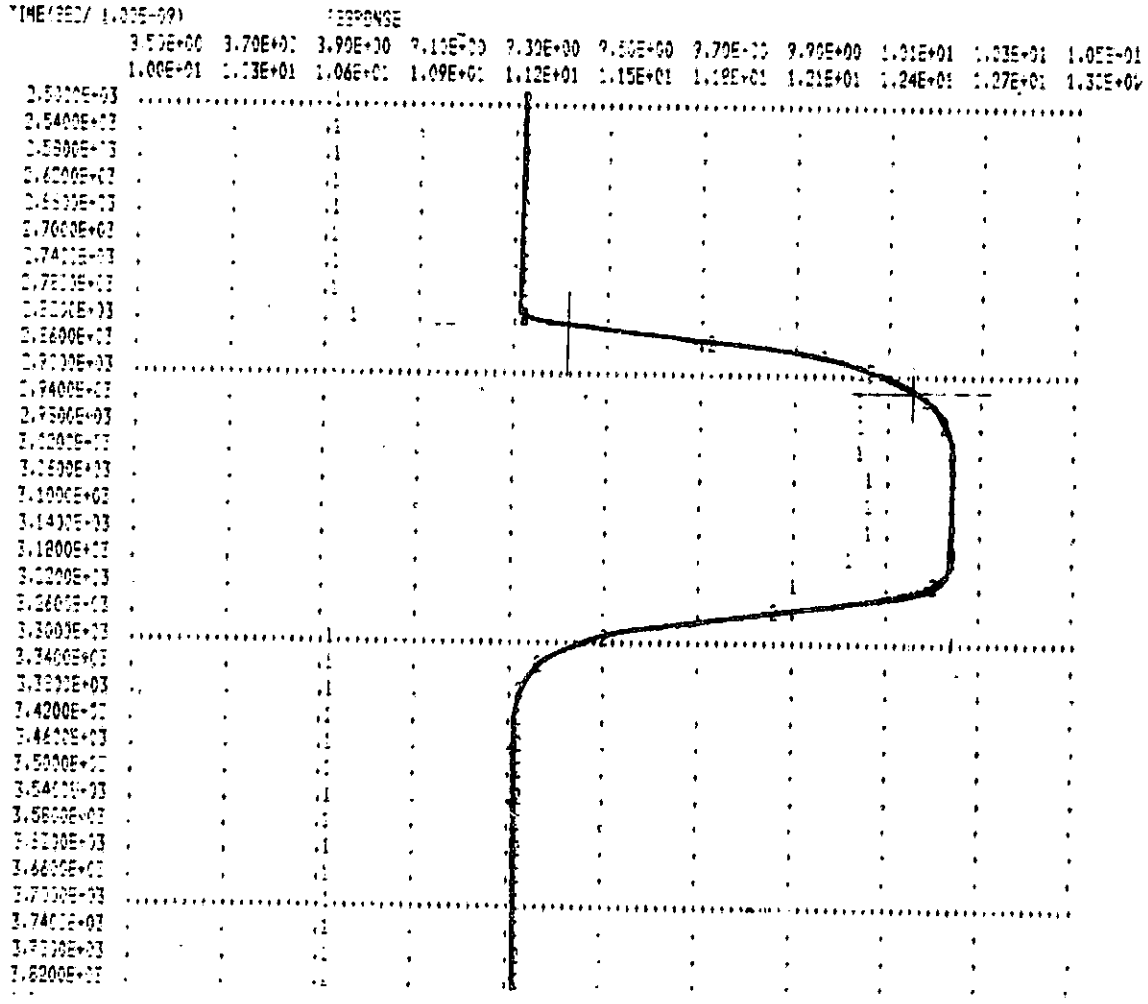
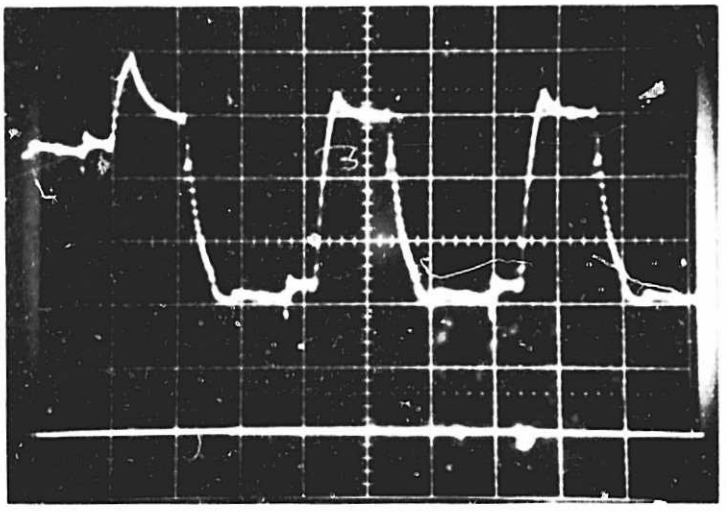


Fig. 4-27. Simulated response for AC input signals.



200 mV/DIVISION 1 μs/DIVISION

Fig. 4-28. Buried-channel floating diffusion amplifier output.

The duplication of the laboratory results using R-CAP provided a starting point for which the minimization of power dissipation was begun. Since the reset FET dissipates negligible power, the single source follower FET configuration shown in Fig. 4-25 was used for the power dissipation tests. The R-CAP parameters channel width (W), channel length (L), and load resistor value were varied to minimize the total power dissipation without unacceptable effects on the gain, fall time, and output impedance. Table 4-15 summarizes the results of this simulation.

The design choice is design number six. This design will give adequate slew rate, good gain, acceptable drive impedance, and a low-power dissipation of 4.1 mW. The design will also provide a WxL product of 110 μm^2 and a layout parasitic value of a = 0.046 pF. Thus, the design will be close to the optimum for minimum FDA noise. This design should give a noise value of 80 rms electrons compared to the minimum attainable, with current design rules, of 71 rms electrons.

4.5.4 Format Conversion

The center tap configuration will provide an interleaved, forward, and reverse video output format. The following discussion describes the output format and addresses both software and hardware methods of format conversion.

TABLE 4-15. SIMULATION RESULTS

Simulation		1 (Test Chip)	2	3	4
W	=	11 µm	5 µm	5 µm	5 µm
(Mask) L	=	10 µm	13 µm	15 µm	15 µm
R_S	=	20K	30K	30K	40K
P-FET	=	2.87 mW	2.55 mW	2.38 mW	1.90 mW
P-Resistor	=	4.37 mW	2.65 mW	2.55 mW	2.10 mW
Total On-Chip Power	=	7.24 mW	5.20 mW	4.93 mW	4.00 mW
Total Power (Buffer (4mW) + On-Chip)	=	11.2 mW	9.2 mW	8.9 mW	8.0 mW
Gain	=	.66	.56	.54	.58
Rise Time @C_S=20 pF	=	165 ns	275 ns	300 ns	388 ns
Fall Time @C_S=20 pF	=	200 ns	350 ns	363 ns	400 ns

Simulation		5	6
W	=	6 µm	6 µm
(Mask) L	=	17 µm	17 µm
R_S	=	30K	40K
P-FET	=	2.55 mW	1.90 mW
P-Resistor	=	2.5 mW	2.19 mW
Total On-Chip Power	=	5.05 mW	4.10 mW
Total Power (Buffer (4mW)+ On-Chip)	=	9.0 mW	8.1 mW
Gain	=	.56	.58
Rise Time @C_S=20 pF	=	300 ns	350 ns
Fall Time @C_S=20 pF	=	340 ns	388 ns

A conceptual view of the CCD imager is provided in Fig. 4-29. Starting from the top it depicts the object that is to be imaged. In this case it is a grey scale with intensity distribution (as seen by each detector) plotted to the right. Next, the line of 512 detectors is depicted with each detector electrically connected to the CCD multiplexer as shown. The CCD multiplexer "T" shape represents the center tap configuration. The numbers and their relative positions in the CCD represent where the information for a given detector is located prior to the dumping of the CCD.

As applied to the computer simulation, each detector variable is assigned a value starting at 0 from detector #1 and increasing linearly to 1 for detector #512. This array of data which simulate a grey scale will be used as the input data for the program. If this data were dumped parallelly into the CCD multiplexer and read serially from one end, the grey scale would be reproduced. However, when the data from the CCD are read from its center via a center tap and alternately read from each side of the center tap, the data are jumbled as shown in Fig. 4-30.

The "scramble" program reproduces this effect. The program defines two counter variables, one for the left side (as viewed in Fig. 4-29) that counts the detector number down from 256 to 1 and one for the right side which counts up from 257 to 512. Knowing that the CCD multiplexer output of the center tap will read alternately from left and right sides starting with the left, the program can use the properties of odd and even numbers to accomplish this effect. Figure 4-31 is the code for this program on the HP-9845 computer.

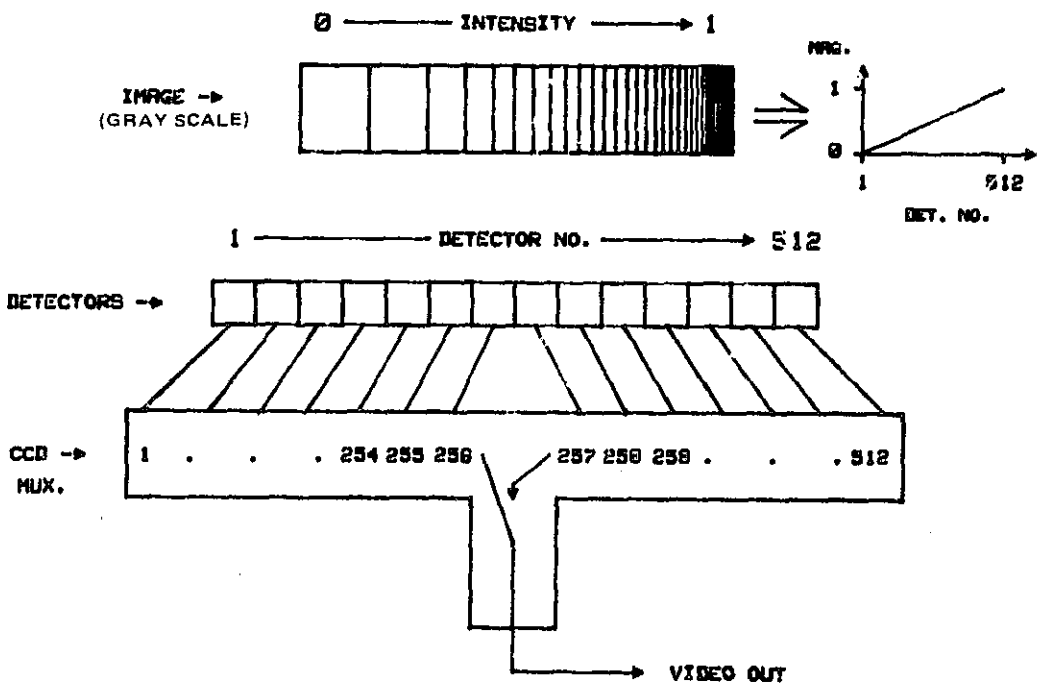


Fig. 4-29. Conceptual view of imager.

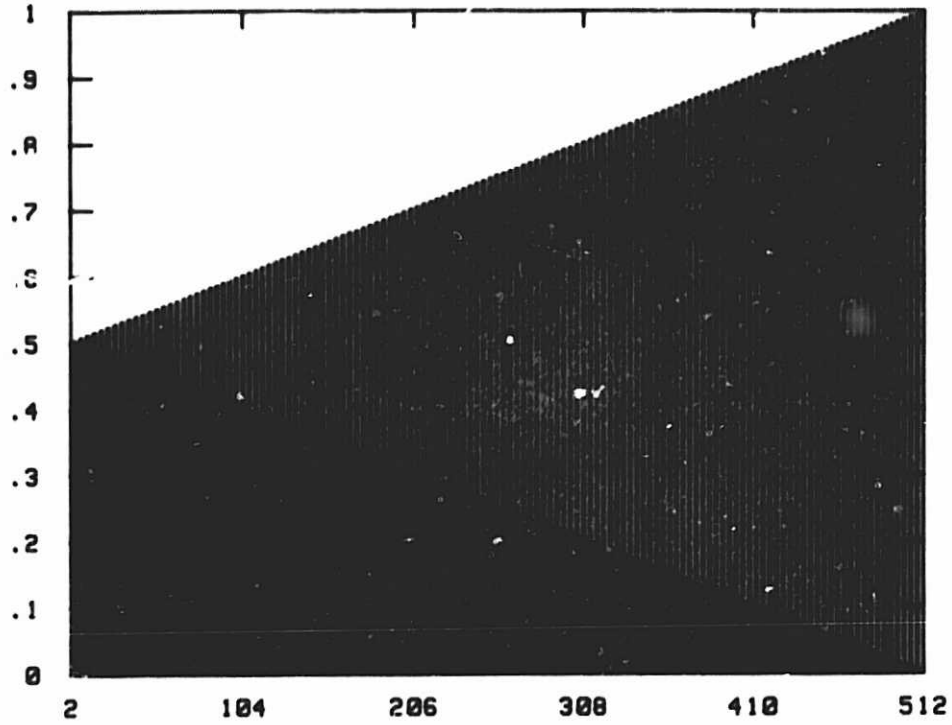


Fig. 4-30. Scrambled from center tap configuration.

```
10    DIM Pix(512)
40    FOR I=512 TO 1 STEP -1          !I DENOTES ORDER OF SERIAL REGISTER DUMP
50    Pix(I)=INT(I/512)               !SET PIXEL LEVEL AMPLITUDE 0 TO 1
70    NEXT I
110   Lside=257                       !STARTING PIXEL NO. ON LEFT SIDE
120   Rside=256                       !STARTING PIXEL NO. ON RIGHT SIDE
130   FOR I=1 TO 512
140   IF INT(I/2)=I/2 THEN GOSUB Right    !IF I IS EVEN
150   IF INT(I/2)<>I/2 THEN GOSUB Left    !IF I IS ODD
151   PRINT Pix_scram                 !VALUE OF CURRENT PIXEL BEING SERIALLY READ
190   NEXT I
200   END
210 Left: Lside=Lside-1               !LEFT SIDE PIXEL NO. COUNTS DOWN 256 TO 1
220   L=1
230   Pix_scram=Pix(Lside)
240   RETURN
250 Right:Rside=Rside+1               !RIGHT SIDE PIXEL NO. COUNTS UP 257 TO 512
260   L=0
270   Pix_scram=Pix(Rside)
280   RETURN
290   END
```

Fig. 4-31. Code for scramble program.

The "unscramble" program essentially uses the same method described for the scrambling program except reversed. The scrambled data are first read from a data file where it had been stored from the scrambling program. The data are read from this data file the way it would be read from the center tap of the CCD multiplexer. The program unscrambles the data and Fig. 4-32 shows the results. The code for this program is in Fig. 4-33.

4.5.5 Unscrambling Electronics Hardware

The data leaving the CCD chip will be digitally converted using an A/D converter operating at a 300K sample/s rate. The data will come in bursts of 512 - 10-bit words representing each dumping of the CCD multiplexer. The bursts will be continuous with no additional time interval between them; therefore, the unscrambling hardware must be able to unscramble one burst of data in the time it takes to dump a data burst from the CCD (512/300K s).

These timing restrictions are dealt with by configuring the hardware into two sections. One section acts as a storage buffer writing the current burst of data to its RAM. Meanwhile the other section is reading the previous burst of data from its RAM using stored decoded address locations read from a common PROM. In other words, the data are read from the RAM in a predetermined order and not sequentially as it was originally written. After each burst, the two sections switch functions. So once section one has written a burst to its RAM it then decodes it while the other section having decoded its data starts to write a new burst to its RAM.

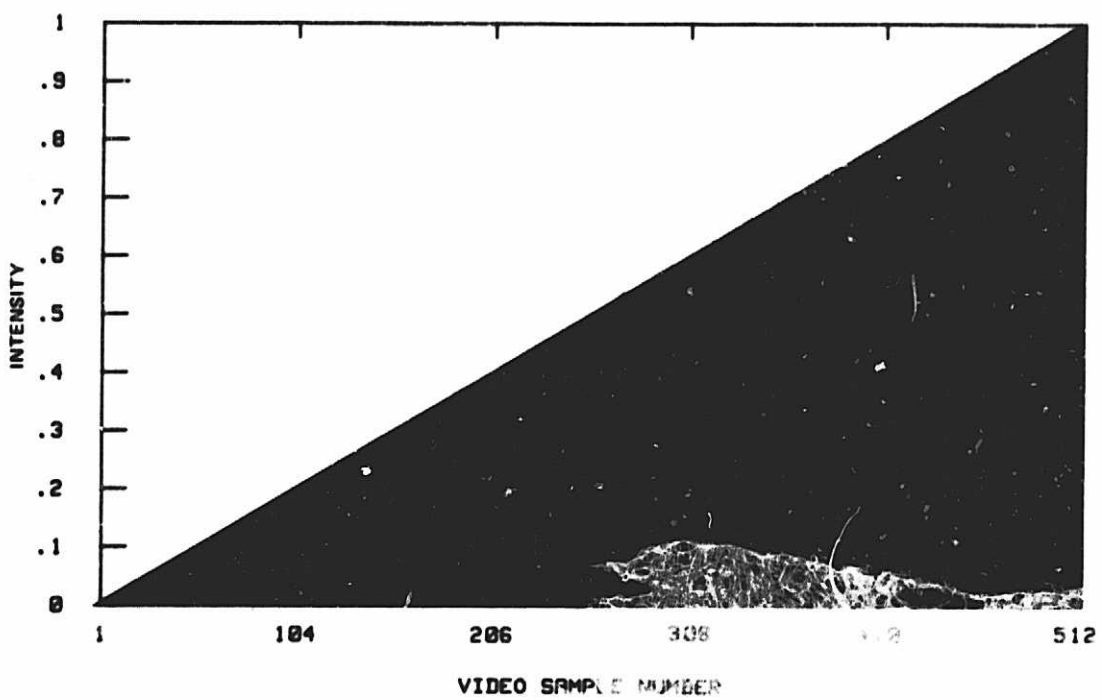


Fig. 4-32. Unscrambled center tap output

```
10     DIM Pix(512)
20     ASSIGN #1 TO "INPUT"
30     PRINT #1;512
40     FOR I=512 TO 1 STEP -1
50     Pix(I)=INT(I/512*1000)/1000
60     PRINT #1;512-I,Pix(I)
70     NEXT I
90     ASSIGN #1 TO "SCRM"
100    PRINT #1;512
110    Lside=257
120    Rside=256
130    FOR I=1 TO 512
140    IF INT(I/2)=I/2 THEN GOSUB Right
150    IF INT(I/2)<>I/2 THEN GOSUB Left
160    IF L=1 THEN PRINT "Pix_scram";Pix_scram;" I=";I;" LEFT=";Lside
170    IF L=0 THEN PRINT "Pix_scram";Pix_scram;" I=";I;" RIGHT=";Rside
180    PRINT #1;I,Pix_scram
190    NEXT I
200    END
210 Left: Lside=Lside-1
220    L=1
230    Pix_scram=Pix(Lside)
240    RETURN
250 Right:Rside=Rside+1
260    L=0
270    Pix_scram=Pix(Rside)
280    RETURN
290    END
```

Fig. 4-33. Code for unscramble program.

In this configuration, each section shares the counter, PROM, address and data lines. This required the use of tristate buffers throughout the circuit and allowed the two sections to be "bi-modal" in operation. A block diagram of the hardware operation is shown in Fig. 4-34.

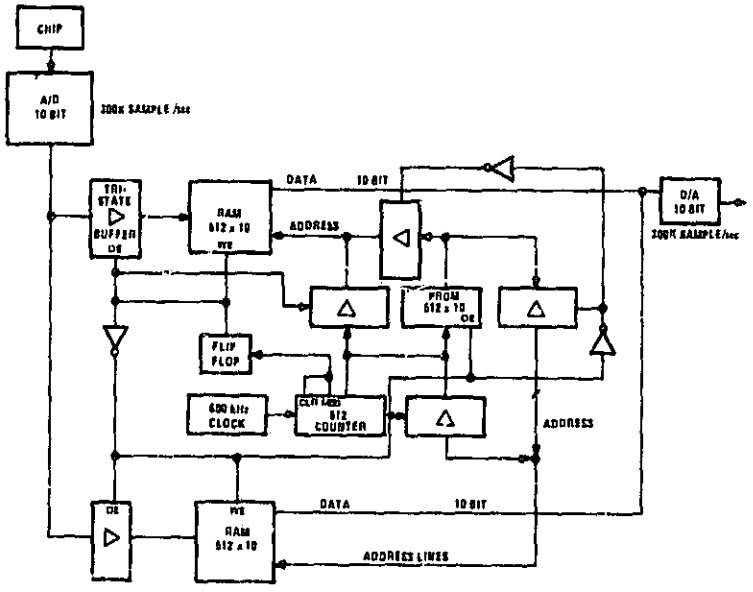


Fig. 4-34. Electronics hardware operation.

4.6 MODULE DIMENSIONS AND BOND-OUT

The module will have an active length of 605 mils. The scribe dimension. before edge definition, will be 625 mils. The module width will be 140 mils. The scribe dimension will be 146 mils. The width of 146 mils will permit adequate space for epoxy mounting to the Test Assembly substrate. For comparison, the TC1258, the 256-detector Schottky device, has dimensions of 75-x-441 mils.

The 625-x-146 module scribe dimensions will permit approximately 48 modules to be fabricated per three-inch wafer (see Fig. 4-35). There will be 22 bonding pads per band or 44 per device. The bond pad designations and location are detailed in Fig. 4-36.

4.7 POWER DISSIPATION

The SWIR module configuration offers high performance at a very low power dissipation. There are three sources of power dissipation on the IRCCD linear arrays. The dominant source is the power dissipation of the two MOSFET output amplifiers. The other two sources are dissipation in the CCD readout registers and dissipation in the Schottky barrier detectors.

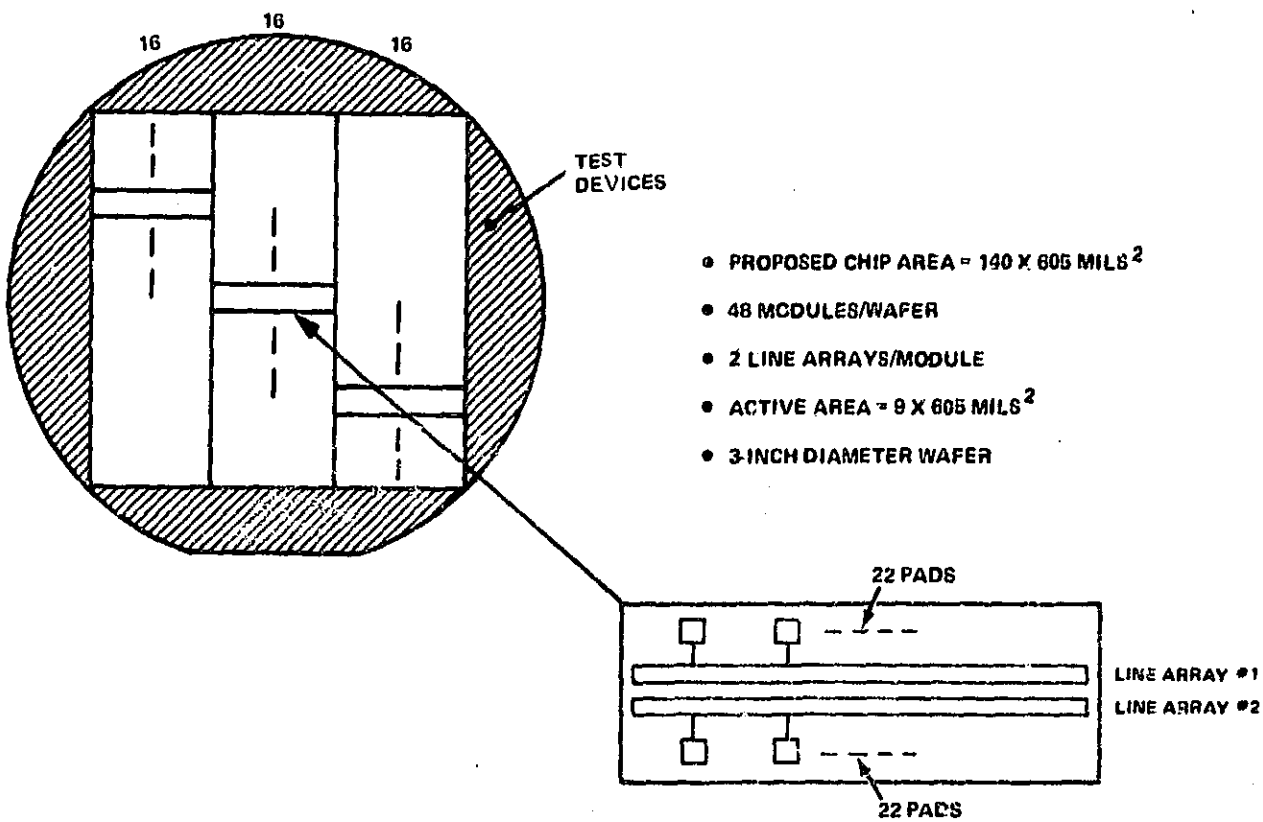


Fig. 4-35. Module density per silicon wafer.

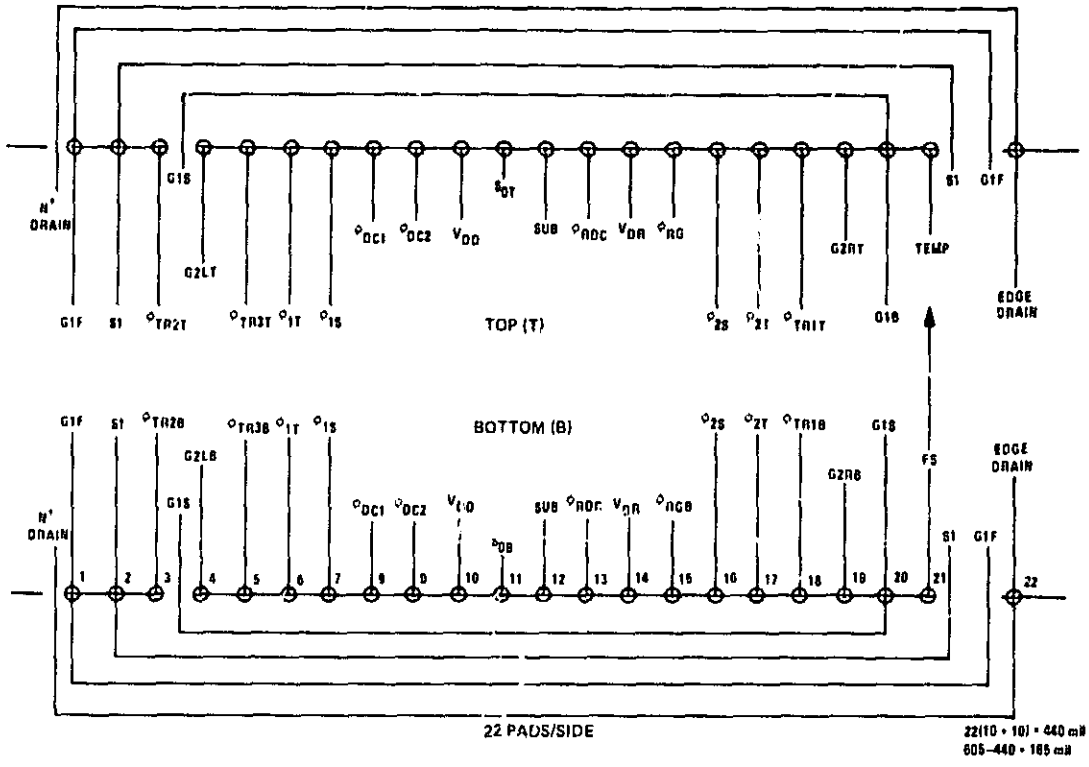


Fig. 4-36. Dual-band sensor bond-out.

The CCD shift registers are buried-channel devices through which signal charge is transported. The charge is moved by appropriate clocking of the directionality controlling polysilicon gates. There are four mechanisms for power dissipation in the CCD register. The first is the power utilized in charging and discharging the resistive polysilicon clock gates. The second source of dissipation is the power used in passing the signal charge through the buried layer, this is effectively a drift current power. The third source of power utilization is that due to lifting the charge packets over the barriers which control the charge packet flow. The final source of power dissipation in buried-channel CCDs is attributed to movement of holes into and out of the depletion region as the registers are clocked.

The power dissipated in the resistive polysilicon gates is dependent upon the clock amplitude and the clock rise and fall times. A derivation of the expression for the gate dissipation is given in the following expression, the numerical values employed are applicable to the final design for the dual-band SWIR sensor.

$$P_{AVERAGE} = P_{PEAK} \times \text{DUTY FACTOR}$$

$$P_{PEAK} = I^2R = \left(\frac{Q}{\Delta t}\right)^2 R N_G$$

$$\text{DUTY FACTOR} = \frac{2\Delta t}{T} = 2 f_c \Delta t$$

$$P_{AVER} = \left(\frac{Q}{\Delta t}\right)^2 R N_G 2 f_c \Delta t$$

C-2

where

R = [25 ohms/square] L_G/W_G

L_G = average transverse length of poly gates (assume 62 μm)

W_G = transverse width of poly gates (assume 10 μm)

Δt = rise, fall time (assume 100 ns)

N_G = number of gates; 4 times number of stages (two-phase clocking; 4-x-512 = 2048/band)

f_c = clock frequency (assume 256-x-1/1.8 ms = 142 kHz)

Q = C_{ox} x V_c (C_{ox} upper bound capacitance)

V_c = clock amplitude (assume 8 V)

C_{ox} = [0.36 fF/μ^2] [L_E W]

L_E = storage length + barrier length (assume 15 μm)

W = stage width (assume 62 μm)

thus

$$P_{AVER} = \frac{C_{ox}{}^2 V_c{}^2 2\, f_c R\, N_G}{\Delta t} \quad \text{(RESISTIVE GATES)} \qquad (4\text{-}18)$$

For the final design the total dissipation due to resistive polysilicon gates is 7.5 μW per band or 7 μW for each module.

The power utilized due to the signal "current" flow is given by the following:*

$$P_{AVER} = \frac{Q_s \lambda^2 f_c{}^2 N_{st}}{\mu_s} \qquad (4\text{-}19)$$

(CURRENT)

*R. Strain, "Properties of an Idealized Traveling Wave Charge Coupled Device," IEEE Electron Devices, vol. ED-19, October 1972.

where

Q_s = signal charge (assume WLI; τ = 1.8 ms, λ = 1.25 μm, 1.41 x 10^5 electrons)

λ = stage length (assume 30 μm)

f_c = clock frequency (assume 142 kHz)

N_{st} = number of stages (assume 512)

μ_s = effective electron mobility [assume 550 $cm^2\ V^{-1}\ s^{-1}$]

For the module design chosen the power dissipation due to signal current is 0.01 μW per band or 0.02 μW for each module.

The third source of power dissipation in the CCD registers is that due to the "lifting" of the charge packets over the clock-induced barriers. An expression for this power dissipation is given by the following:

$$P_{AVER\ (TRANSPORT)} = 2\ Q_s\ f_c \left[V_b + V_{AV} - \frac{Q_s}{2\ C_p} \right] N_{st} \qquad (4\text{-}20)$$

where

V_b = barrier height (assume 8 V)

V_{AV} = average driving voltage above V_b (assume 2 V)

Q_s = signal charge (assume τ = 1.8 ms, λ = 1.25 μm, 1.41x10^5 electrons)

C_p = storage gate capacity (assume maximum, C_{ox})

C_{ox} = [0.36 fF/μm^2] [L_E W]

L_E = storage length + barrier length (assume 15 μm)

f_c = clock frequency (assume 142 kHz)

N_{st} = number of stages (assume 512)

For the final design the dissipation due to charge transport is approximately 0.05 mW per band or 0.1 mW for each module.

The final source of shift register power dissipation is due to the movement of holes into and out of the depletion region as the buried channel is clocked. This charge movement is supported by the substrate power supply through the resistive substrate. The amount of charge flow (holes) is dependent upon the

clock amplitude and the clock bias, as well as, the amount of signal charge. The following is an expression for the substrate dissipation due to the movement of holes into and out of the depletion region:*

$$P_{AV\ (SUBSTRATE)} = 2\ C_D\ V_D^2\ f_c\ N_S \qquad (4\text{-}21)$$

where

C_D = $[0.07\ fF/\mu m^2][L_R\ W]$

V_D = $[0.96\ V_c] - [0.98\ Q_s/C_c]$

C_c = $[0.18\ fF/\mu m^2][L_R\ W]$

Q_s = signal charge (assume τ = 1.8 ms, λ = 1.25 μm, 1.41×10^5 electrons)

V_c = clock amplitude (assume 10 V)

L_R = half the stage length (assume 15 μm)

W = stage width (assume 62 μm)

f_c = clock frequency (assume 142 kHz)

N_S = number of stages (assume 512)

For the final design the dissipation due to depletion region clocking is 0.85 mW per band or 1.7 mW for the module. The total CCD register dissipation is thus anticipated to be approximately 1.8 mW for the chosen module design. This is equivalent to 1.75 μW dissipation per pixel.

The Schottky barrier detector dissipation will be very low. The sources of power dissipation in the detectors are leakage current power and the power involved with vidicon mode transfer from the detector to the CCD register. The leakage current is so low that this dissipation will be negligible. The power involved with vidicon mode transfer will be small. As an upper bound on this dissipation assume that all the CV^2f energy involved in the reset operation is dissipated as real power. Therefore, for the final design the detector dissipation must be less than the following:

$$P_{MAX\ (DETECTOR)} = C_{DT} V^2\ f_T\ N_{st}$$

*The quantitative data used in this and other formulas were derived from a buried-channel CCD model created by RCA Laboratories and ATL. These parameters reflect the nominal buried layer and depletion region characteristics.

where

C_{DT} = detector capacitance (assume 0.063 pF)

V = reset clock amplitude (assume 10 V)

f_T = parallel transfer frequency (assume 1/1.8 ms = 556 Hz)

N_{st} = number of detectors

For the module design the detector dissipation will be less than 1.8 μW per band or 3.6 μW for the module. Thus, the detector dissipation is negligible.

The dominant power dissipation source is the buried-channel MOSFET amplifiers. The simulated power dissipation is 4.0 mW per amplifier or 8.0 mW for the module. To this dissipation the hybrid buffer dissipation must be added. The current design for the buffer calls for a power dissipation of 4.2 mW for each 2-transistor buffer, or 8.4 mW to support the dual-band module design.

The total power dissipation for the dual-band 2-x-512 design with the center tap configuration and on-hybrid buffers is summarized in Table 4-16. The total power dissipation is thus 18.2 mW for each module.

TABLE 4-16. MODULE POWER DISSIPATION

Dissipation Source	Dissipation per Module	Dissipation per Detector
CCD Register Resistive Gates	7 μW	7.0×10^{-3} μW
CCD Register Signal Current	0.02 μW	2.0×10^{-5} μW
CCD Register Transport	0.1 mW	9.5×10^{-2} μW
CCD Register Depletion Dissipation	1.7 mW	1.8 μW
Schottky Detectors	3.6 μW	3.5×10^{-3} μm
MOSFET Amplifiers	8.0 mW	7.8 μW
Amplifier Buffers	8.4 mW	8.2 μW
TOTAL	18.2 mW	17.8 μW*

*RFP specification for power dissipation is ≤ 26.8 μW.

4.8 RADIATION EFFECTS

The effects of radiation on the operating characteristics and performance of the Schottky barrier IRCCD technology should be acceptable for a 5-year MLA mission. Two investigations into the effects of radiation have been undertaken to date. The first analysis and experimentation were performed during the MLA instrument definition studies. Prior to the SWIR contract award, a second experimental investigation had also been initiated. The second study involves the placement of a Pd_2Si focal plane and test devices in the NASA Long Duration Space Exposure Experiment (LDSEE). The following discussion reviews the findings to date and details RCA's participation in the LDSEE study.

The Schottky barrier IRCCD technology should exhibit good radiation tolerance. MLA Instrument Definition Studies and preliminary experiments indicate that for a 5-year MLA mission, the performance will be slightly degraded. However, if certain operational conditions are met, the performance will stay within the limits of calibration capability.

The principal reason that there is not a large degradation in performance is that the MLA environment is rather benign. First of all, the maximum expected total ionization dose of 6×10^3 rads(Si)* is a factor of two below the range where MOS devices commonly start to show appreciable effects. Furthermore, the absence of fast neutrons assures that there will be no appreciable displacement damage.

However, because of the low-temperature (120°K) operating environment, there will be greater than normal (298°K) flat-band voltage shifts induced by the ionizing radiation. After analysis of the findings in the literature, it appears that there could be a 1- to 3-V shift in the CCD operating potentials. This assumes little or no annealing. In actuality, it is quite likely that at 120°K the self-annealing process will keep pace with the slow radiation accumulation process. If not, exposure to 200°K to 250°K temperature periodically would improve the annealing rate (perhaps that is inevitable if the passive cooler is to undergo a periodic burn-off purge).

The radiation effects on CCDs and NMOS transistors at room and cryogenic temperatures are well known and understood. The only aspect of the SWIR sensor which is not thoroughly understood in the context of radiation effects is the Pd_2Si detector. To gain a better understanding, a 32-x-64 area array (Pd_2Si) was bombarded with ionizing radiation. The purpose of this experiment was to measure the operating characteristics before and after radiation and thereby determine radiation effects.

The experiment was conducted at the Cobalt-60 Radiation Laboratory at the RCA Solid State Division, Somerville, NJ. A device from wafer 11G-14 was exposed to radiation levels of 5000 rads (Si) while all CCD, and other accessible gates, were tied to positive +5 volts bias. The IR radiation was

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*Ball Aerospace assessment.

done at room temperature. After irradiation, a 230-mV threshold shift was observed in the output amplifier active-load device (V_{GG} = 1.25 → 1.01). The Schottky-diode transfer-gate threshold change was 720 mV (V_T = 8.03 → 7.31). With the identical bias as before exposure, the vertical ("B") register exhibited poor transfer efficiency; however, with some bias adjustment acceptable imagery was achieved.

The Schottky detector dark-current level (at 125°K) seemed to vanish completely following irradiation. This is an important observation because increased detector dark current was the degradation phenomena of concern. It thus appears that the detector exhibits radiation tolerance. At 300°K the output ("C") register had large CCD dark current (~ 1/2 full well), but at 125°K the CCD dark current vanished.

The MOS threshold shift (V_{GG}) and the Schottky vidicon transfer gate shift (V_T) were small enough that no adjustment was needed to make corrections for radiation effects. However, as indicated in Table 4-17, the CCD threshold shifts were appreciable.

TABLE 4-17. RADIATION TOLERANCE FOR SCHOTTKY BARRIER DETECTORS

V_{MB} (Volts)

	$V_{pinning}$		$V_G = 0$	
	Poly 1	Poly 2	Poly 1	Poly 2
Before →	-6.5	-12.0	-6.5	-10.8
After →	-1.5	- 6.8	-1.3	- 4.8
ΔV_{MB} →	5.0	5.2	5.2	6.0

Operational Bias (Volts)

	V_{GG} (THRES)	V_T (THRES)	ϕC1,3	ϕC2,4	G_4	G_5	G_6
Before →	1.24	8.03	-15.66	-6.40	7.10	13.86	19.59
After →	1.01	7.31	-19.71	-8.87	3.15	16.80	19.59
ΔV_{TH} →	0.230	0.720	4.05	2.47	3.95	2.94	0

Most probably, a satellite system would require bias adjustment over the life of the mission to accommodate the dose accumulation. An important observation should be made, however. The V_{MB} shift in pinning voltage and in offset were approximately the same for both first and second level polysilicon gates. This means that a minimal number of independent bias adjustments would be needed.

During the third quarter of 1982 RCA delivered two packaged integrated circuits to the Georgia Institute of Technology for inclusion in the Long Duration Space Exposure Experiment (shuttle launch and retrieval experiment, nominal 6-month orbit in space). The responsible project leader at Georgia Tech is Dr. Donald Blue. The integrated circuits were (1) a 32-x-64 Pd_2Si focal plane array and (2) an IRCCD process test device test key. Prior to delivery, the Pd_2Si 32-x-64 array was completely characterized for operating potentials, blemish characteristics, transfer efficiency, noise, and response uniformity. The test key was characterized for NMOS threshold voltages, NMOS transconductance, and CCD V_{MG} potentials. Mechanical samples of the IC packages have previously been sent to assure mechanical compatibility between the IRCCD test samples and the LDSEE mechanical design.

It has been agreed that after the LDSEE capsule is recovered from space, RCA will measure the IC performance and furnish a report to Georgia Tech on the effects of space exposure on device performance. This experiment, while not a rigorous investigation of radiation effects, will give a first look at the real effects of the space environment on Pd_2Si IRCCD technology.

4.9 MODULE THERMAL PROFILE

An extensive multinode analysis of the temperature distribution on the silicon detector module was accomplished during the MLA Instrument Definition Study. As part of the SWIRS design study the analysis was reviewed and updated. The objective of this analysis was to determine the degree of approach to isothermality of the line array of detectors. The specific cause for concern about the departure from isothermality was the dissipation in the FET amplifiers. The goal of this analysis was to determine if the on-chip dissipation disturbed the isothermal nature of the detectors in the regions near the amplifiers. Furthermore, it was desirable to know the average-module temperature rise.

The analysis was done using a 378-node thermal model. The model represented the silicon module affixed by conductive epoxy to an isothermal surface (this would be the package substrate). The 3-dimensional model represented the dissipation zones as separate rectilinear solids, each of uniform heat flux. The model accurately represented the placement and dissipation magnitude of the proposed amplifier, detectors, and CCDs. The epoxy bond was considered to be 4 mils thick with 70% area coverage (K_{EPOXY} = 0.053 W/in-°K conductivity). A 30-mil package window (slit) was included in the modeling. The thermal conductivity of silicon at 100°K was used, rather than the room temperature value. It turns out that the thermal conductivity at 100°K is approximately three times as great as it is at 298°K (K_{Si} = 17.8 W/in-°K at 100°K).

The result of the analysis was very favorable. Table 4-18 summarizes the expected temperature rise above the isothermal surface at various points along the detector array, and at the amplifier locations. The results presented in the table are for the center tap configuration with the single-stage on-chip amplifier. As may be seen, the "hottest" spot on the chip, the area containing the output amplifier transistor, is only 0.40°K above the isothermal package substrate temperature. Looking at all the detector locations, the largest temperature differential along the detectors is only .034°K. Thus, there will be negligible

TABLE 4-18. MODULE TEMPERATURE RISE ABOVE PACKAGE SUBSTRATE

Selected Locations	Temperature Rise (°K)
Amplifier Drive Transistor	0.4010
Detector #248	0.3786
Detector #250	0.3799
Detector #252	0.3808
Detector #254	0.3815
Detector #256	0.3816
CCD Stage #250	0.3799
CCD Stage #252	0.3809
CCD Stage #254	0.3821
CCD Stage #256	0.3822

detector dark current differentials caused by temperature nonuniformity. Furthermore, the heat flux will be very uniformly distributed. This fact coupled with a substrate package design of high-conductivity silicon will result in a very small module temperature rise (<1°K) above the temperature provided by the TA cold finger.

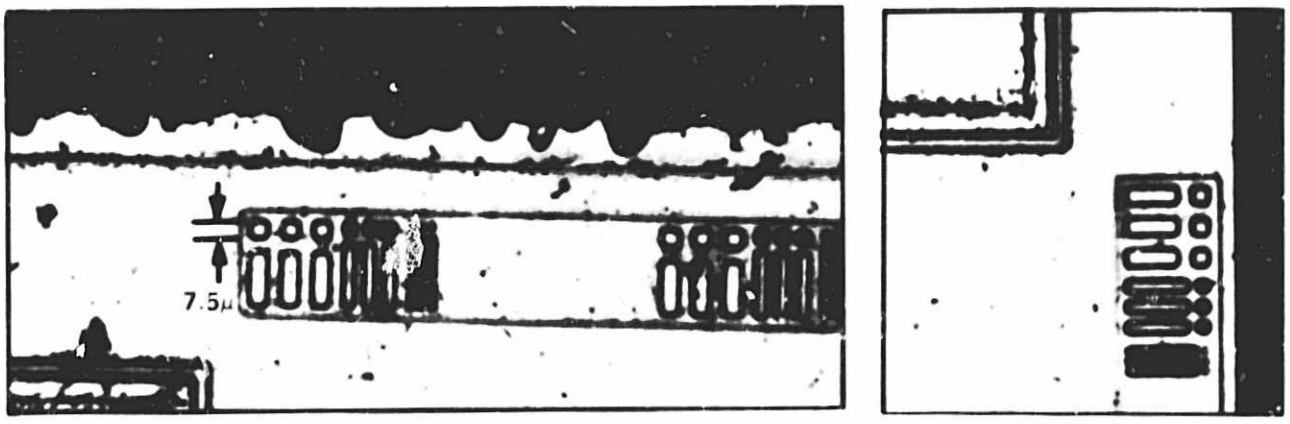
4.10 EDGE DEFINITION TECHNIQUE DEVELOPMENT

As previously stated, mechanical end-to-end butting is the preferred butting technique. In preparation for end-to-end alignment, the module abutment edges must be precisely defined with minimal damage to the active devices. Candidate edge defining procedures include anisotropic plasma etching, wet chemical etching, sawing, polishing, and combinations of these techiques. The results to date of an on-going investigation into edge definition techniques are presented in the following discussion.

During the RCA portion of the MLA Instrument Definition Study, the sawing and polishing technique was investigated. The test vehicle was a fully processed RCA visible-light photocapacitor array. This array formed a chip size of approximately 500 mils by 80 mils if chips were taken in pairs. The 2-inch silicon wafer (16-mil thickness) was first diamond sawed to produce the 500-mil-by-80-mil pieces of silicon (this size is comparable to the dual-band chip size). After diamond sawing, the chip edge (80-mil edge) looked as shown in Fig. 4-37a. The degree of chipping may be ascertained from the fact that the square dot on the largest triplet of the resolution patterns (square over a rectangle) is nominally 0.3 mils (7.5 μm).

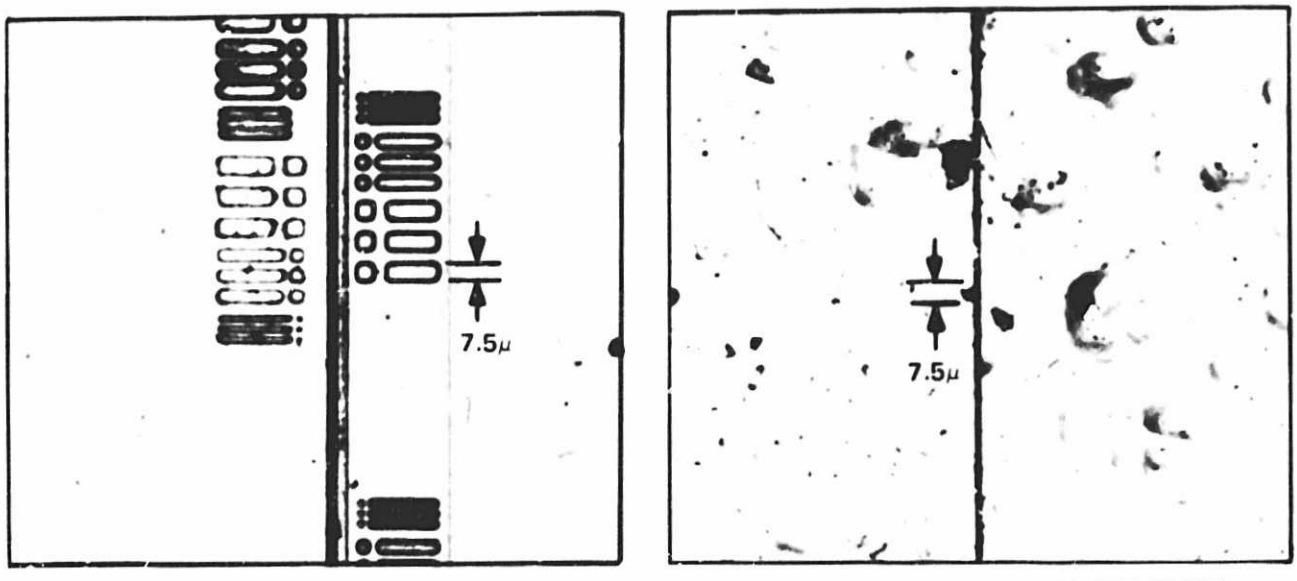
The next step was to polish (lap) the chip edge. This was done using a polish that is similar to that used for polishing the back surface of the Schottky IRCCD wafers. A polished edge looks as shown in Fig. 4-37b. The edge after polishing is very smooth, with negligible surface damage, and has very accurate orthogonality to the chip structure (no skew).

The final test of this technique was the actual placement of two chips end-to-end after polishing. As may be seen in Fig. 4-38, the results were



(a) AFTER SAWING (b) AFTER POLISHING

Fig. 4-37. Abutment edge after conventional sawing.



(c) TOP VIEW (200 X) (d) BOTTOM VIEW (PRIOR TO CLEANING)

Fig. 4-38. End-to-end abutment shows on accurate end match with only a 6-μm gap.

very good. The gap between the chips on both the top and bottom was on the order of 0.24 mils (6 μm). While this technique provided excellent results with respect to physical characteristics, this experiment yielded no data on electrical degradation. The question of leakage current increase due to mechanical damage was not addressed by this investigation.

From this starting point another set of experiments was initiated. The purpose of these experiments were (1) to look at new approaches to low-damage, precision edge definition, and (2) to measure the magnitude of the electrical damage due to sawing. It was decided that thin-silicon CCD imagers laminated to a glass substrate would be used as the test vehicle. Since this is the technology to be used for the Visible/Near IR Development and this edge definition is more demanding than the SWIR all-silicon definition problem, the results of the development effort should provide edge definition solutions for both imager technologies.

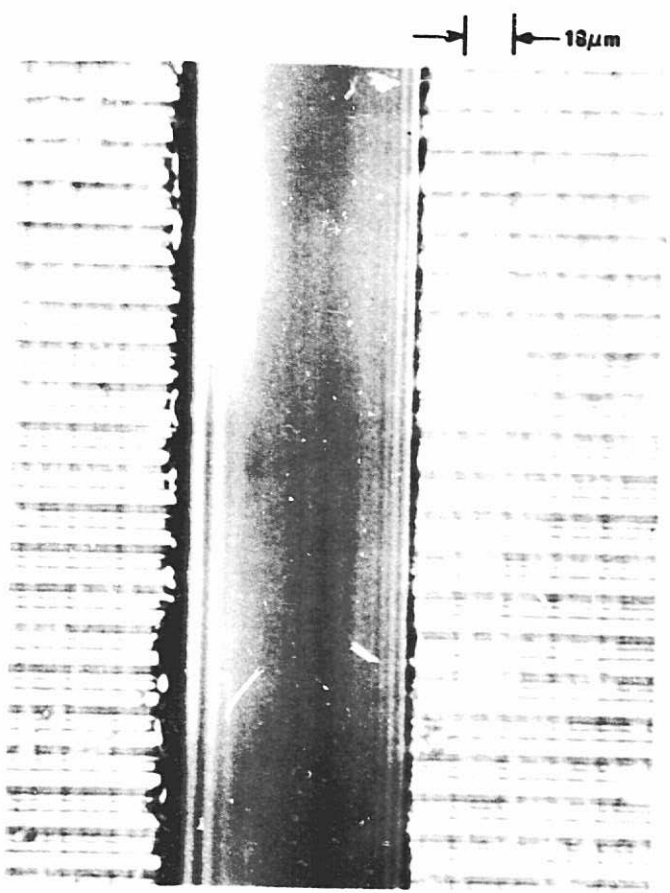
At RCA Laboratories, thin glass-laminated wafers on which there are three fully processed CCD imagers have been used for a series of sawing tests to determine the edge quality that can be obtained using a Tempress 604 saw. Resin-bonded blades three mils thick and having 9-μm diamond grit have produced cut edges with discontinuities (chips) in the silicon structure extending no further than 5 μm from the cut edge over distances of several millimeters. When the laminated wafer is waxed to a thick Si support to supply greater rigidity during the sawing operations and the cut depth is greater than the 25-mil thickness of the laminated structure, the edge quality is that shown in Fig. 4-39a. This thin sawing disc is normally mounted in a chuck which exposes only 10 mils of the blade. Blade breakage is high, so thicker blades with fine grit will be employed in the future. Most of the cuts have been only part way through the glass laminate.

Figure 4-39b shows the minimum gap obtained when two cut edges such as shown in 4-39a were brought together. The gap is 8 to 8.5 μm wide over a distance of 3 to 4 mm. As can be seen, a lot of dirt is present along these edges, the residue from having mounted the samples in a wax to permit microscopic examination of the cut edge, so the gap width may well be narrower when clean samples are used.

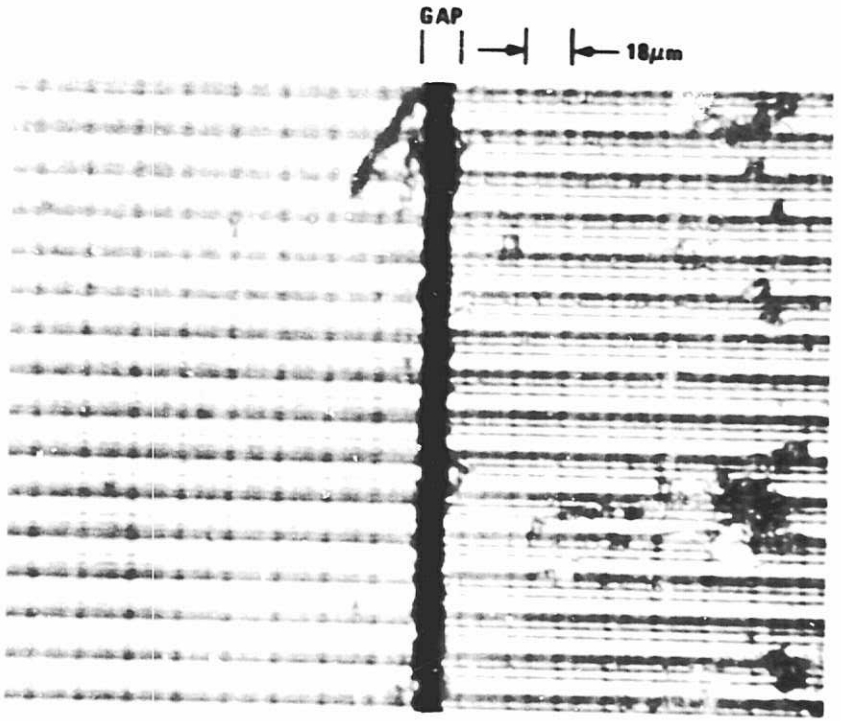
These sawing tests are very encouraging and appear to show that little or no polishing will be required for the butt edge of the VIS/NIR or SWIR devices, if the proper blades and cutting speed are employed.

More recently an overlayer of clear wax has been applied to the surface of the wafer after it has been waxed to the thick silicon support. This overcoat has reduced chipping of the silicon and provides a mask for subsequent etching of the exposed edges of the saw cut.

The effect of sawing on the electrical performance of a CCD structure is the subject of another investigation. Operable frame transfer imagers were identified by probe testing of processed wafers (fabricated in Lancaster, PA) operating at standard TV rate. A saw cut is made at right angles to the gate lines extending



- THIN SILICON ON GLASS AFTER SINGLE CUT
- 3 MIL RESIN BONDED BLADE WITH 9μ DIAMOND GRIT
- TEMPRESS 605



- ABUTMENT SEAM GAP $<9\mu$
- EDGE CHIPPING LIMITED TO $<5\mu$

Fig. 4-39. Silicon sawing experiments.

from the top of the image register to the center of the storage register. The device will still image in the storage register because the gates are double-end connected. However, since the clocking of this register is interrupted only during the retrace intervals of the TV scanning cycle, operation with strobe illumination at field rate is required. Prior to sawing, the dark current of each operable device (there are three devices per wafer) was measured on the probe station and imaging characteristics of the storage register illuminated by a strobed image were noted. After sawing, the electrical performance of devices was again examined. Dark current increases of 10^3 to 10^4 were observed in all samples. A silicon etch which does not attack the BPSG overlayer protecting the device was shown to be effective in reducing the dark current to a level about 10X the original. Results have been variable and in only half of the devices was the dark current lowered sufficiently to obtain imaging operation. The best sample has a region on each side of the saw cut in which several vertical CCD columns are saturated with dark current. Shown in Table 4-19 is the dark current history for two sawed devices on one wafer.

The initial dark current reduction resulting from etching is not stable. Coating the etched silicon edge with wax has overcome this instability, and in some cases has further reduced the dark current. Despite the presence of both a surface wax layer and the BPSG surface layer on the device, there is evidence that a long duration etch extends several micrometers away from the cut edge without providing further reduction of dark current.

TABLE 4-19. SAWED IMAGER OPERATING AT TV RATE

	Dark Current Chip 1 (A)	Dark Current Chip 3 (A)
Initial	$.8 \times 10^{-8}$	$.65 \times 10^{-7}$
After sawing	$.8 \times 10^{-4}$	1×10^{-4}
After etch	1×10^{-7}	8×10^{-7}
After waxing exposed edges	6.4×10^{-8}	5.3×10^{-7}
After heating 120°C, 40 min	6×10^{-8}	1.5×10^{-7}

The most recent saw cuts have been terminated in the middle of the image register where there is an antiblooming structure separating the CCD columns. If we can successfully wire-bond across the sawing gap in the gate line bus bars of this register, it should be possible to evaluate the effect of having a variation in the wafer doping adjacent to the edge pixel.

Another approach by which we expect to provide samples with a change in doping in the region of the saw cut will be a test structure included in the mask set for a new device design. Samples will be available in the near future.

Experimentation to reduce the dark current introduced by the raw edge of the saw cut and to provide stable passivation is being continued. It is felt that precision sawing, followed by lapping and appropriately masked passivation etching will provide the final, successful edge definition technique.

4.11 MASK LEVELS FOR THE Pd_2Si – FPA FABRICATION

The mask levels for the dual-band module will be essentially the same as those utilized on the 6-x-128 high-density imager. The dual-band sensor mask levels are listed in Table 4-20.

TABLE 4-20. DUAL-BAND SENSOR MASK LEVELS (TA11567)

Designation	Mask Level	Priority	Tone
M1	Alignment Mask	1	Dark Field
M3	Channel Stop (P^+)	1	Clear Field
M4	Thick Oxide	1	Dark Field
M6	BCCD Implant (I) - [N Type SBD Guard Rings for Low Fill-Factor; Amplifier + CCD Register]	1	Dark Field
M7	Poly 1	1	Clear Field
M8	Poly 2 (I) - [Low Fill-Factor SBD Poly Isolation]	1	Clear Field
M10	N^+ Diffusions (Incl. SBD)	1	Dark Field
M11	Implanted Guard Rings (I) - [Poly Isolation, Low Fill-Factor]	1	Dark Field
M19	Schottky Contacts (I) - [Low Fill-Factor]	1	Dark Field
M21	Aluminum [All Metal, Incl. Reflectors]	1	Clear Field
M23	Pads	1	Dark Field
M25	BCCD Implant (C Register)	1	Dark Field
M28	Contacts (Reg., Not Incl. SC)	1	Dark Field
M32	SiO [Both Bands for Cavity]	1	Dark Field
M33	Passivation Etch Mask	1	Dark Field
M34	BCCD Implant (II) - [N Type SBD Guard Rings, High Fill - Factor; Amplifier + CCD Register]	2	Dark Field
M35	Poly 2 (II) - [High Fill - Factor SBD Poly Isolation]	2	Clear Field
M36	Implanted Guard Rings (II) - [Poly Isolation, High Fill - Factor]	2	Dark Field
M37	Schottky Contacts (II) - [High Fill-Factor]	2	Dark Field
M38	SiO - [Single Band for Cavity]	1	Dark Field
M39	BCCD Implant (III) - [No SBD Guard Rings; Amplifier + CCD Register	2	Dark Field

TABLE 4-20. DUAL-BAND SENSOR MASK LEVELS (TA11567) (Continued)

Designation	Mask Level	Priority	Tone
M40	Aluminum - [Same as M21, But No Reflectors]	2	Clear Field
M41	Aluminum - [Reflectors Only]	2	Clear Field
M92	SiO [Both Bands for Cavity]	1	Clear Field
M98	SiO [Single Band for Cavity]	1	Clear Field

4.12 SUMMARY OF DUAL BAND SPECIFICATIONS

Table 4-21 summarizes the dual band sensor specifications. The sensor will have two linear arrays with 512 detectors each. The cross-track spacing will be 30 μm center-to-center. The along-track spacing from band-to-band will be 300 μm (10 IFOV). The fill-factor will be 48-68% for the conservative design approach and 75-83% for the aggressive design approach. One of the bands will be optimized for operation in the 1.25-1.65 μm spectral region. The other band will be optimized for operation at 2.22 μm.

TABLE 4-21. BUTTABLE DUAL BAND SENSOR SPECIFICATIONS

Number of Detectors	2 x 512
Cross-Track Pitch	30 μm
Along-Track Spacing	300 μm
Detector Fill-Factor	68-83%
Quantum Efficiency Goals	
λ = 1.25	20%
λ = 1.65	14%
λ = 2.22	5.5%
Charge Capacity	1.1×10^6 e
Operating Temperature	120-125K
Dark Current (120K)	2nA/cm^2
Noise Floor (rms)	100-117 e$^-$
Pixel Loss at Seam	2

The read-out mode for each band will be a once per frame parallel transfer from the detector/parallel transfer region to the serial CCD registers. The two serial CCD registers of each band have a shared, center tap floating diffusion amplifier output. The amplifier is a single on-chip buried channel FET source follower. This amplifier will be connected to an on-focal plane buffer for the Test Assembly implementation. The serial CCD registers have electrical input ports. All the CCD registers are fabricated with N-buried channel, double polysilicon gate technology.

Resident on the module will be test diodes, test amplifiers, process test devices and a temperature sense diode. The dual band sensor will have 22 bond pads per band, for a total of 44 for the module.

Section 5

TEST ASSEMBLY DESIGN

5.1 PACKAGE DESIGN

The primary packaging goals are precision and stability over the wide temperature range, with good thermal conduction from the modules. Primary goals direct the design toward the use of a single material with a minimum number of firmly anchored interfaces between module and cold sink. The package must also provide electrical, mechanical, and optical interfaces to the focal plane.

The test assembly (TA), shown in Fig. 5-1, consists of a polycrystalline silicon substrate carrying a two-layer thick-film interconnecting conductor pattern and five modules epoxy mounted in precise contiguous relationship. The substrate has a baffled aperture exposing module photosensitive areas to focused radiation. The modules are connected with wire bonds to substrate metalization which extends to the substrate edge for solder connection to ribbon cables. Also included in the assembly are chip capacitors and resistors for optimum circuit bypassing and electrical trimming. A polycrystalline silicon cover enclosing the modules and fragile bond wires will, after prototype evaluation, serve as a radiation and EMI shield, thermal conductor, and contamination seal. The silicon cover would be sealed to the substrate with berylia-loaded epoxy to provide electrical insulation from the input/output conductors and good thermal conduction across the joint. During prototype evaluation, the thermal and mechanical mounting surfaces will be 1-x-2-inch unpopulated regions at opposite ends of the test assembly substrate.

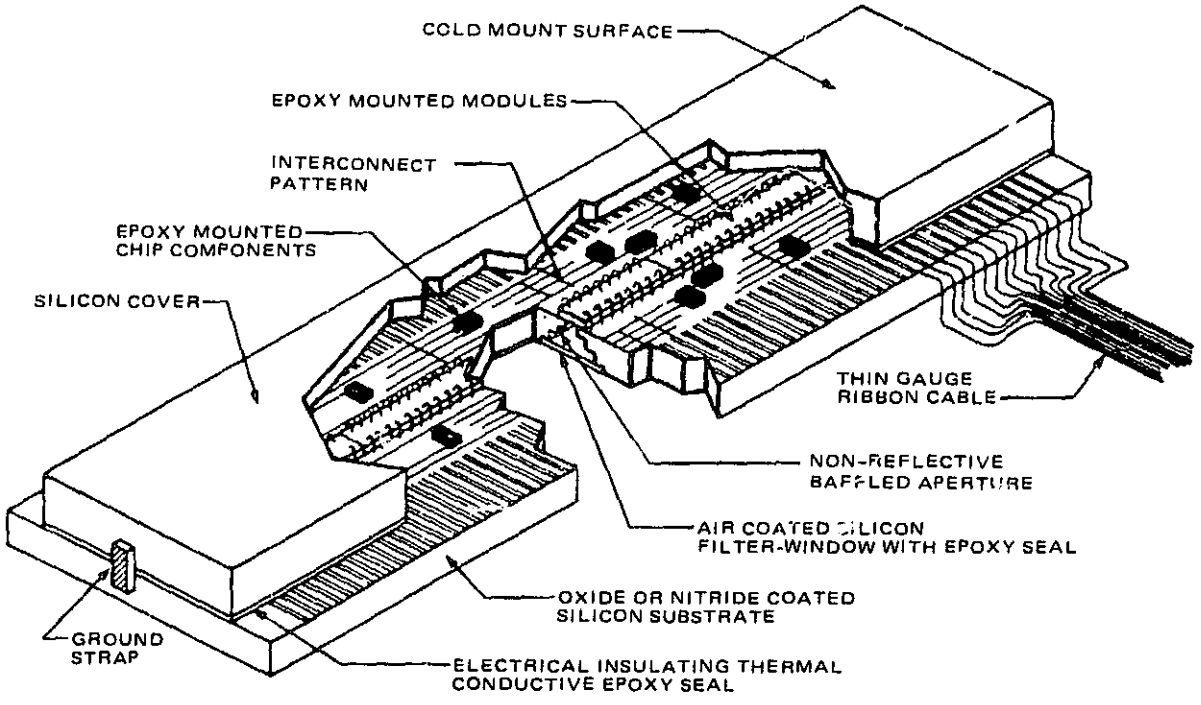


Fig. 5-1. Focal plane concept.

The design trade study was directed toward proving the novel features of the TA design. The use of silicon as a packaging material and as a substrate for thick-film circuitry was investigated and will continued to be investigated. Details of module alignment and component mounting are currently under study.

5.1.1 Package Design

To avoid thermally induced strains resulting from the approximately 200K swing from room ambient to operating temperature, the substrate must closely match the coefficient of thermal expansion (CTE) of the silicon modules. Mismatches over the anticipated temperature range will result in bimetal distortion, and, in the extreme, crashing of adjacent modules if clearances are very small. Silicon uniquely combines perfect CTE match, high thermal conductivity at 120K (equal to silver), low density and high modules. The undesired features of silicon for this application are difficult fabrication and brittle fracture. These problems are being addressed.

Silicon wafers (3-inch diameter by 15-mil thickness) were subjected to repeated thermal shock tests by immersion in liquid nitrogen at about 77K. Wafers survived six immersions and returned to room ambient without any visible degradation.

Silicon blocks 2-x-4-x-1/4 inches were also thermal shock tested successfully. Because of silicon's notch sensitivity, the test was repeated with a silicon block 2-x-4-x-1/4 inches with a slot 100 mils wide by 3 inches long centrally located through the 1/4-inch thickness. The slotted block survived without visible degradation.

Our vendor had no trouble machining the slot using a diamond saw plug cut and finishing the ends with a diamond end mill. No problems have been encountered in handling the silicon slabs during thick-film printing and testing, adding to our confidence that silicon is an acceptable package material for this application.

5.1.2 Thick Film on Silicon

Substrate metalization could in principle be either thin film or thick film. The requirement for insulation of two-level metalization combined with the need to match the CTE of silicon led us to prefer thick film. However, there is no reported experience in thick-film materials fired on silicon outside of solar cell fabrication where it is used for contacts through oxide or nitride passivation. As a consequence we have requested Electro Science Laboratories (ESL) to develop materials for this application.

Most thick-film materials have been developed for use on substrates made with high alumina (i.e., 96 or 99.5%). Variations of these compositions have been adapted for use on other substrates such as berylia, procelain-enamel coated steel, stabilized zirconea, and soda-lime glass. Considerable difficulties in formulating thick films arise when the use of substrates lower in CTE than alumina are proposed. Thus, hard borosilicate glasses, silicon, and quartz substrates represent greater degrees of difficulty, in inverse relationship to their decreasing CTE values.

Among these last three substrate materials, silicon, in particular, adds an additional degree of difficulty in that it is not an electrical insulator. Shorting between printed conductor lines can occur even when oxide or nitride films are deposited on the silicon.

This was confirmed by initial insulation tests using silicon dioxide as the insulating medium. Silicon wafers with a 0.015-inch thickness and a 3-inch diameter were oxidized to a 1-μm thickness. A conductive gold pattern using ESL 8835-1B material was fired on the wafer. Massive shorts ensued.

A second test was made using conventional materials. A single layer of dielectric, ESL 4612, was deposited and then followed by a gold-stripe pattern using ESL 8835-1B gold. Both were fired in air at 805C.

The second test was very encouraging in that only a small number of shorts occurred, approximately one line in ten. The lines were 10 mils wide and 900 mils long.

This second sample was dipped in liquid nitrogen (LN) and returned to room temperature (RT) several times. The material remained adherent and the number of shorts did not increase. These tests justified the development of materials matched to the silicon substrate characteristics. Electro Science Laboratories undertook this task.

The problems addressed during the design trade study were first, to electrically insulate a silicon substrate without significantly increasing the thermal resistance through the insulating layer. Once having achieved that, the second objective was to deposit a conductive gold interconnect pattern which would not short to the substrate through the initial insulation or passivation layer. The third objective was to develop a dielectric isolation composition which will allow two-level gold conductor layers to be formed for interconnecting the Schottky barrier infrared detector modules.

The solutions to these problems involved the development of the desired materials in thick-film screen print and fire form. A carefully matched glass system (ESL 4478, glaze) was applied for the silicon passivation layer. It was formulated to deposit only a 3- to 4-μm (0.12 to 0.16 mils) thick fired film when printed through a 325-mesh stainless steel screen. This unusual thickness can be compared to the normal thick-film glass pastes which typically deposit single fired layers between 12 and 18 μm (0.5 to 0.7 mils).

Single and double prints of ESL 4778 were printed and these were fired for 12 to 15 minutes at peak temperature (980 to 1000C) resulting in a smooth, glassy, pinhole-free layer on the silicon. For initial test, 3-inch-diameter silicon wafers 38 μm (15 mils) thick were used for substrates.

The glaze, developed by Electro Science Laboratories (ESL 4778), was carefully formulated to have a coefficient of thermal expansion (CTE) very close to that of silicon, 36×10^{-7} cm/cm/°C. It was fired, in air, at 980C, to a thickness of 5 μm.

The wafers with the fired glaze were repeatedly thermal shocked by immersion into liquid nitrogen. No detrimental effects were observed.

Subsequently a two-layer circuit, as well as a crossover test pattern, were fired upon glazed wafers. The pastes used were both developed by ESL for use on silicon, 8841 gold and 4779 crossover dielectric. All firing was done at 850C in air. A schematic cross-section is shown in Fig. 5-2.

The mechanical and electrical properties of the insulating pastes are listed in Tables 5-1 and 5-2. The gold, 8841 has a resistivity of 3.5 to 4 milliohms per square for a 5-μm-thick film.

Wire bondability tests were performed on the gold using both thermosonic (heated stage 100C) and pulsed thermocompression bonding (work at RT). Both types of bonding were satisfactory and met or exceeded the MIL-specification strength for the size wire used (0.001-inch-diameter gold).

The stencil screens used were 325-mesh stainless steel wire 0.0011-inch diameter and emulsion thickness of 25 μm for the crossover dielectric. The passivation screen was the same except that only a base coat emulation was employed. The emulsion thickness for the gold conductors was 15 μm.

A slab of polysilicon 2 inches by 4 inches by 0.25 inch was obtained. Upon it was fired the two-layer test circuit previously mentioned. The screening and firing parameters were the same. Capacitors and integrated circuits were mounted as discussed in Section 5.1.6 (see Fig. 5-3). Thermosonic wire bonding was used for connections to the semiconductors.

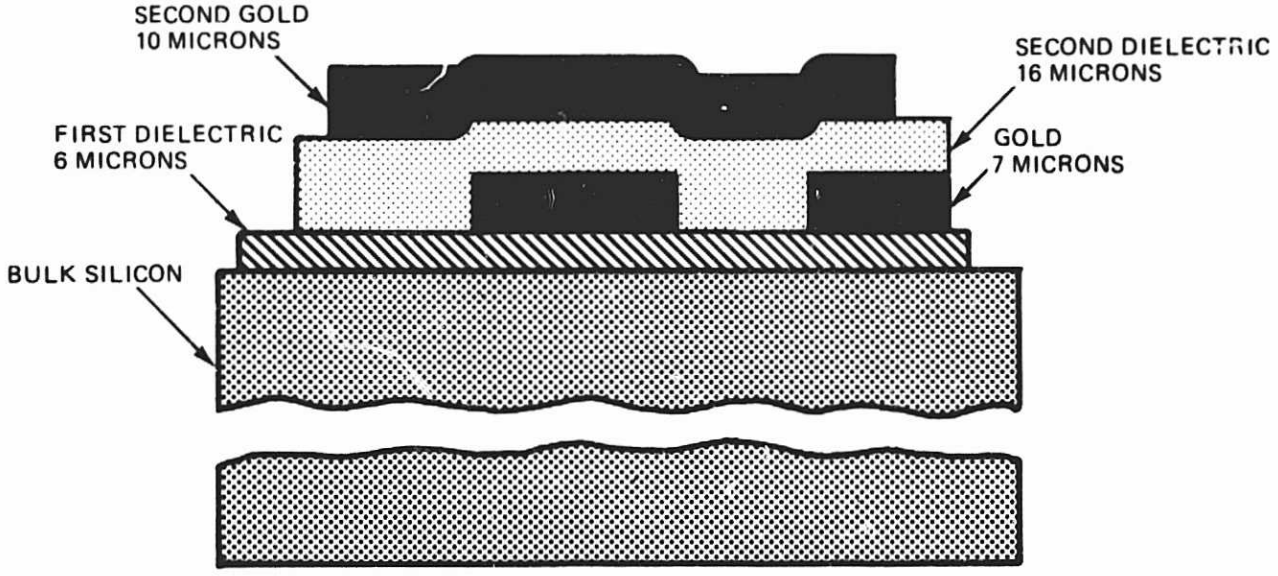


Fig. 5-2. A schematic cross-section of the thick-film hybrid structure.

TABLE 5-1. MECHANICAL CHARACTERISTICS OF HYBRID MATERIALS

MATERIAL	TYPE	BROOKFIELD RVT PASTE VISCOSITY 10 RPM	CTE ($\times 10^{-7}$ cm/cm/°C)	BURN-OUT TEMP °C	TOTAL FIRING TIME (minutes)	PEAK TEMP, °C
#4478, GLAZE	VITREOUS	50 ± 10 KCPS	35-37	300-450	60-80	980
#4779 DIELECTRIC	DEVITRI-FYING	190 ± 20 KCPS	39-41	300-400	40-50	850

TABLE 5-2. ELECTRICAL CHARACTERISTICS OF HYBRID MATERIALS

MATERIAL	DIELECTRIC CONSTANT (1 kHz)	DISSIPATION FACTOR (1 kHz)	INSULATION RESISTANCE AT 50 VDC (25 μm)	BREAKDOWN VOLTAGE (25 μm)
#4778	10-12	0.5 - 0.7%	3×10^{11} ohms	400
#4779	18-21	0.2 - 0.4%	1×10^{11} ohms	500

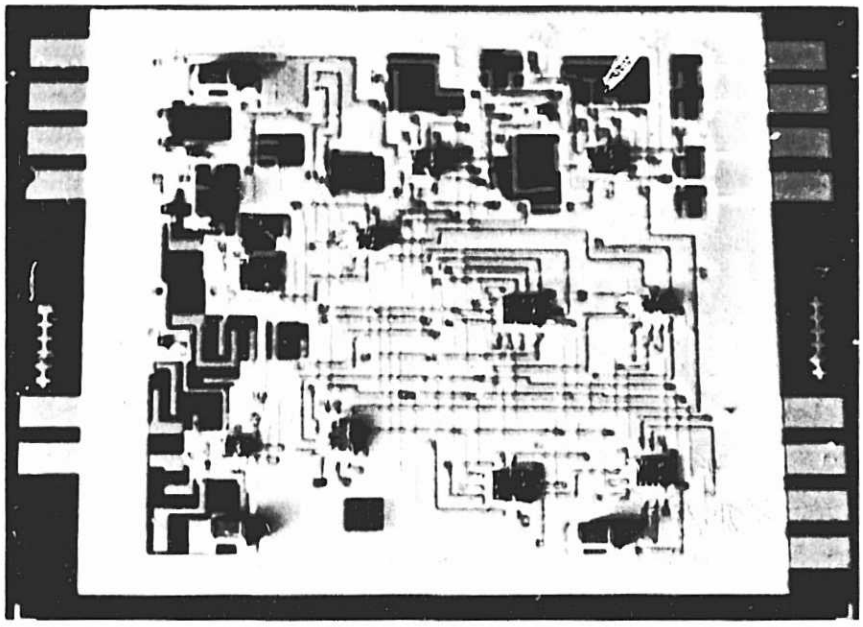


Fig. 5-3. The test hybrid used to test thick-film technology.

These thick substrate assemblies were thermally shocked by immersion into liquid nitrogen. All of the epoxy-mounted components remained firmly attached with no apparent difficulties.

Wire-bond adhesion tests were conducted on the circuit to check for any change due to the thermal shock. A small difference was observed between those wires attached to the first metal (next to the passivation glaze) and the metal on top of the crossover dielectric. The sample size was limited.

Microscopic examination revealed microcracks in the crossover dielectric, but at magnifications up to 1000X the conductor traces appeared undamaged. After observing the microcracking, a new formulation of the dielectric was requested from ESL. This insulator has recently been demonstrated as the solution to the microcracking problem.

A second slab of polysilicon was obtained with a 0.100-inch-wide slit machined into it. The 3-inch slit extended to within 1/2 inch of the ends of the slab. This simulated the type of slit which will be in the final package for mounting the sensor arrays. Thermal shocking of the slab was by direct immersion into liquid nitrogen. No detremental effects were observed.

5.1.3 Module Alignment

The alignment of modules is accomplished using a glass optical flat as a transfer fixture. The modules are manipulated to precise position one at a time with the metalized face down in contact with the fixture. Upon attaining correct position, each chip is clamped securely by increasing the slight vacuum that is applied during manipulation. The full complement of modules is then transferred to the substrate using epoxy mounting.

The optical flat surface provides planarity reference while X- and Y-alignment is achieved by registering module alignment targets against etched chrome reticle lines 10 μm wide (0.4 mil) on the transfer fixture. A layout of the module alignment marks is shown in Fig. 5-4. The marks are placed on the metalization layer of the module a sufficient distance from the active area to prevent any interference with operation.

An inverted split-field microscope is used to observe registration at two extremes of the module simultaneously. As indicated in schematic form in Fig. 5-5, the inverted microscope and illuminator are attached to the vertical ways of a Bridgeport milling machine base. The Bridgeport base with X, Y, and Z movements forms a massive, stable foundation for the alignment operation.

To manipulate the modules into registration, a micropositioner is used. Precision antibacklash slides with differential micrometer drivers and a precision goniometer provide fine translation in X and Y directions and rotation about the Z-axis.

Modules must be held by the micromanipulator firmly in the X and Y directions to avoid backlash during operation, but the hold must be compliant in the Z direction to allow the module to rest on the reference flat. Module restraining options include vacuum, magnetic, electrostatic, and mechanical means.

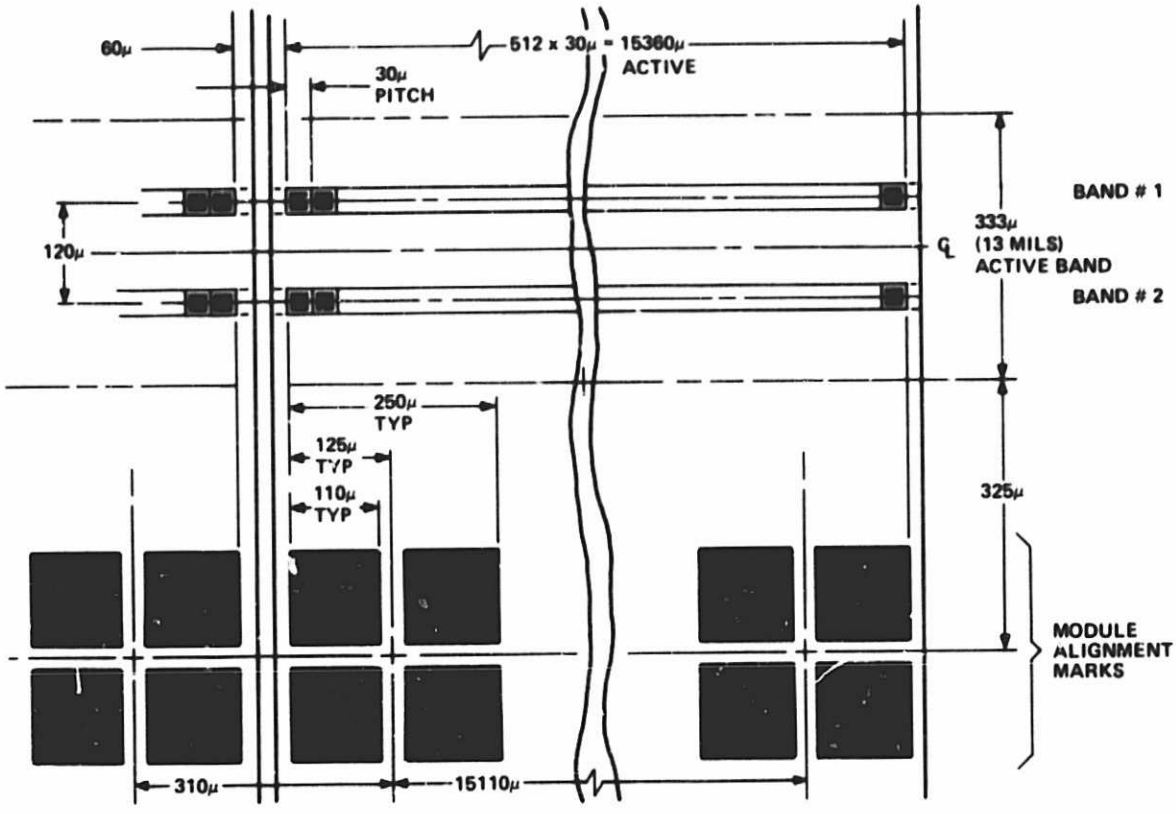


Fig. 5-4. Module alignment for two-pixel loss.

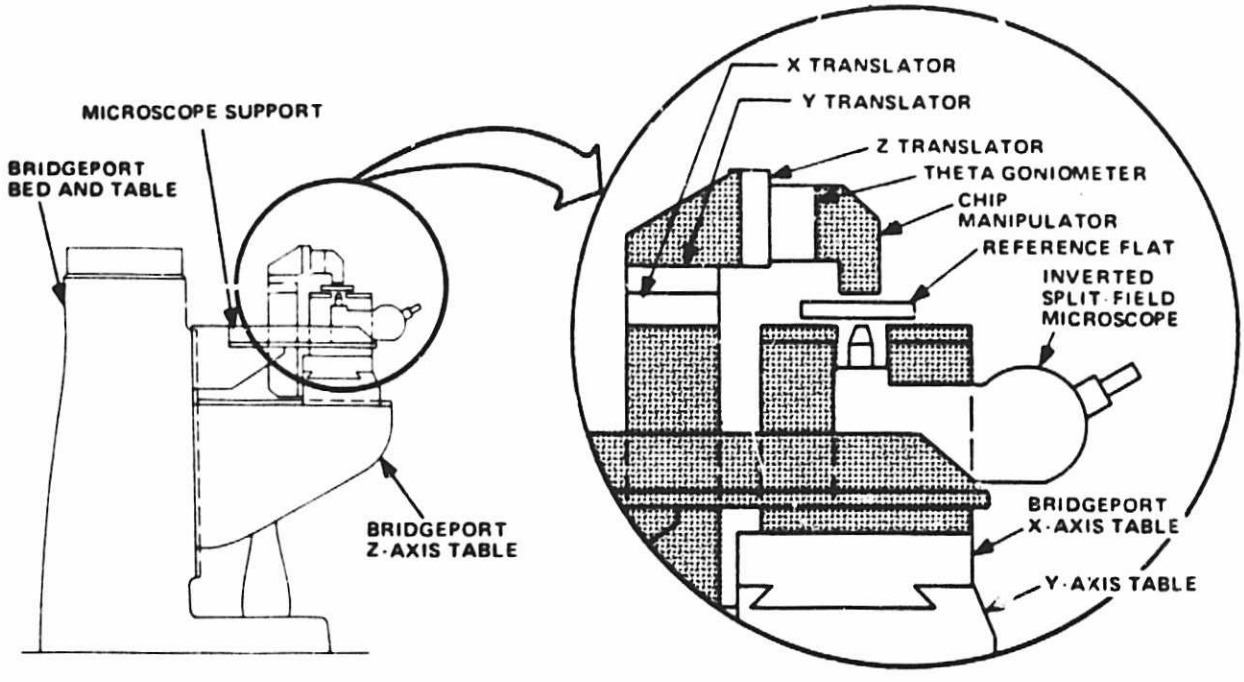


Fig. 5-5. Alignment equipment.

The vacuum method is currently being tested because it offers several advantages for this application. Vacuum clamping is potentially free from backlash and releases without perturbing the module. Electrostatic clamps expose the module to undesired fields. Magnetic gripping is feasible but requires application of magnetic material to the module which is unnecessary with the vacuum clamps.

A brassboard testing was designed and is being fabricated. The objective is to determine the design details which combine desired stiffness in the X and Y directions with compliance in the Z-axis and a firm grip on the module.

We are also generating a layout using a Bridgeport milling machine base as a stable foundation. The Bridgeport base was delivered in early February.

The split-field microscope is another essential component for module alignment. We are considering the relative merits of products from Unitron, Zeiss, and Suss. The decision will be based on inverted configuration, minimum interobjective spacing, working distance and field-of-view at 100X, overall vertical dimension under objective, general optical performance (e.g., flat-field, freedom from distortion, etc.), and cost.

5.1.4 Module Replacement

The ability to reclaim a reject focal plane by removing and replacing a defective module is cost effective only if (1) the process imposes a modest penalty on normal yield and performance, and (2) the repair is accomplished at a small fraction of original focal plane cost. The following paragraphs describe a concept for attaining these objectives.

5.1.5 Module Removal

Basic design of the focal plane remains as described. Only the pattern of the mounting epoxy is altered to facilitate module removal. To minimize risk of damage to adjacent modules, the areas under each module near the butted ends (about 20 to 25 mils) are maintained clear of epoxy. After manual removal of bond wires from the defective module, it is possible to cut through most of the module thickness using the diamond wheel as shown in Fig. 5-6. When the module has been cut to within 3 to 5 mils of the bottom with ample clearance to adjacent modules, the underground ends are broken free by careful manipulation of a manual tool using magnification. The remainder of the module and most of the mounting epoxy are removed by further grinding to present an acceptable surface for module replacement.

Mounting epoxy is applied to the substrate using a stylus and then the replacement module is manually placed in approximate position on the epoxy. The new module is close to the correct position on the X-axis (due to guidance from adjacent modules) but is not algined in the Y-axis and projects above the focal plane.

A variation of the original alignment procedure is used for replacement. A spectral optical reference flat and manipulator is required. The reference flat carrying reticle lines extends the full length of the focal plane but is only about 0.09 inch wide to contact module faces while clearing wire bonds as shown in Fig. 5-7. The reference flat is manipulated to align its reticle with the replacement module which is then locked to the flat by vacuum. The flat and replacement module are moved as an assembly to align the reference flat with the remaining

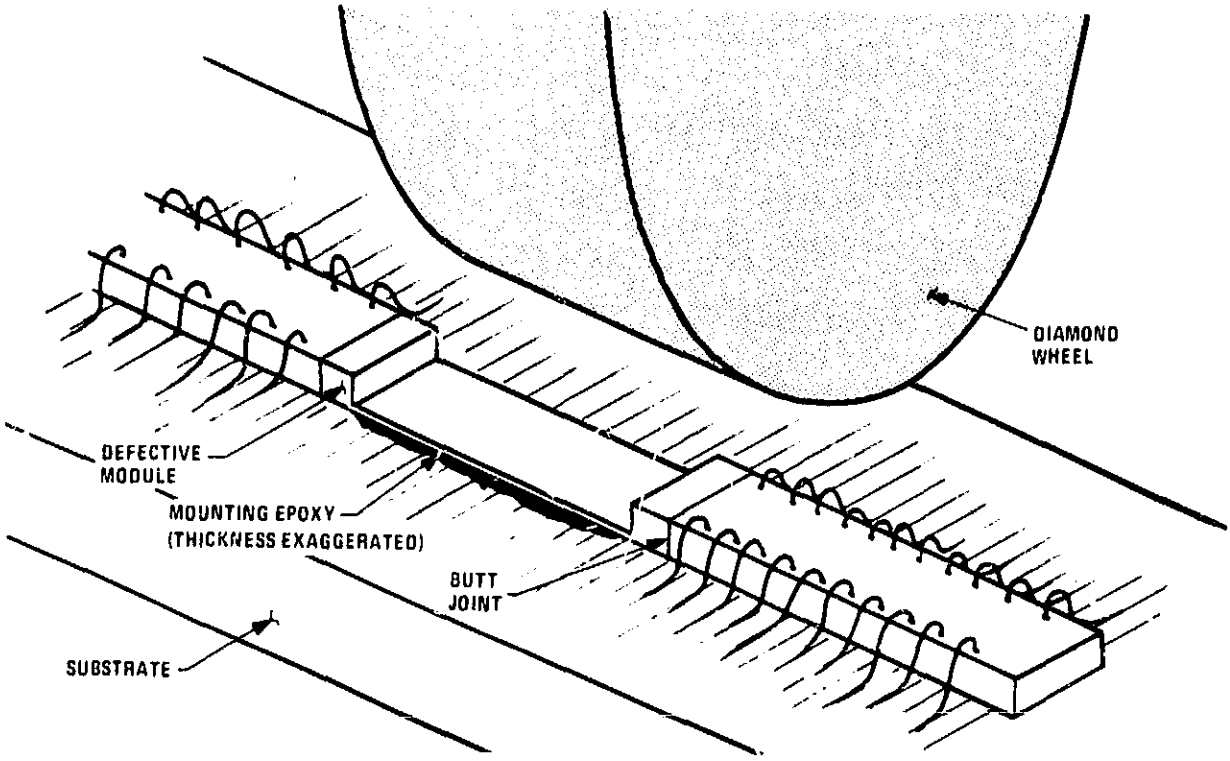


Fig. 5-6. Module removal scheme.

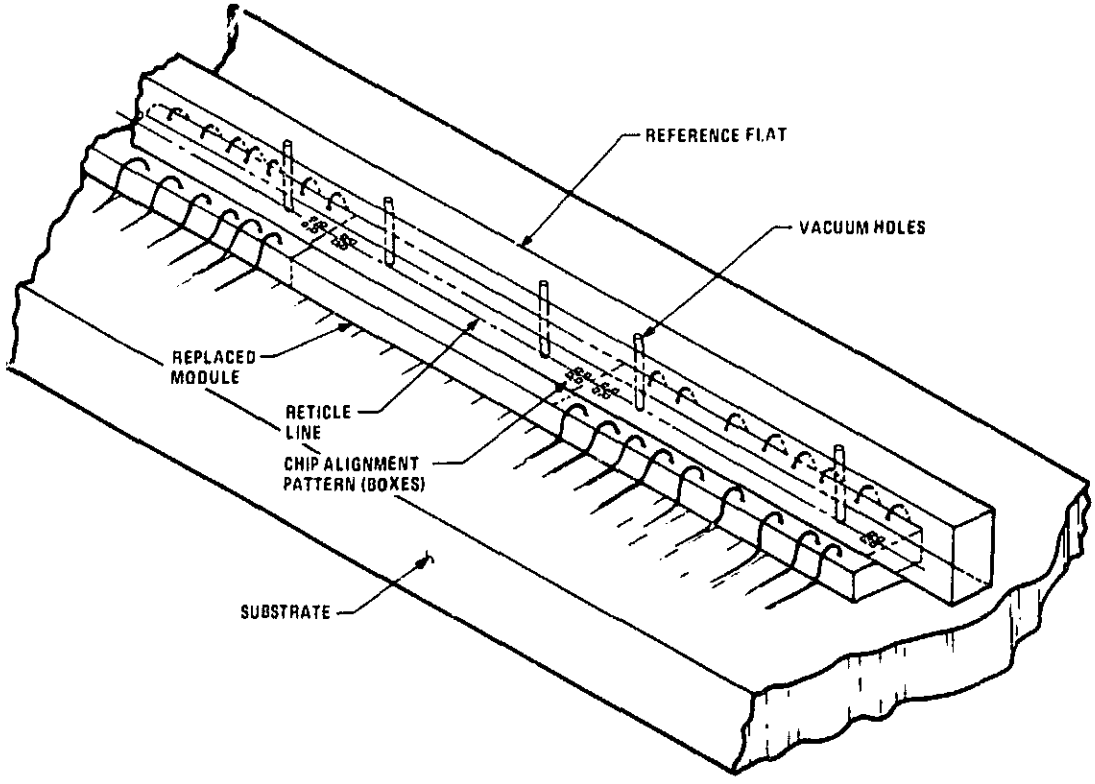


Fig. 5-7. Replacement module alignment.

modules. Pressure applied to the flat will then assure module coplanarity as the epoxy cures. After epoxy curing at room temperature, wire bonds are applied to the new module.

5.1.6 Component Mounting

Both active and passive devices used with these fired-film-on-silicon substrates are mounted with epoxies. Depending upon the device requirements either a silver filled epoxy for conductive situations or a ceramic filled epoxy for insulating applications is used.

Chip resistors are used instead of fired resistor films printed directly on the silicon substrate. This choice is dictated by the fact that the presently available fired-film resistor materials have their coefficient of thermal expansion (CTE) matched to alumina. Thus, if used directly on silicon substrates, severe cracking would occur.

The conductive epoxy, EPO-TECH H31D, has been used for mounting both active and passive devices. It is a silver filled material.

Thermal shocking of mounted components (resistors, capacitors, and ICs) appeared to cause no damage. The epoxy joints did not crack nor crumble and there were no visible degrading effects; therefore, the chip resistors and chip capacitors pose no reliability problem when mounted in this fashion.

The H31D material is a single component material which cures at 100 to 125C. The cured material is free of outgassing under vacuum conditions.

5.1.7 Component Replaceability

Components mounted with conductive epoxy, H31D, are readily replaceable. A long history of such replacement occurred in the ceramic hybrid applications.

A heated helium gas torch equipped with a small nozzle is used to heat the devices to be replaced. At temperatures of approximately 250C the epoxy adherence to the gold or dielectric material is weakened to such a degree that the part may readily be removed without damage to the circuit.

A new component may then be mounted. The curing temperature, 100 to 125C, is within the storage temperature characteristics of the remainder of the circuitry.

Helium is used as the working medium for the gas torch. The rate of heat transfer using helium is much more rapid than air or nitrogen. The inert atmosphere is a bonus, but the primary reason for the helium gas is the enhanced heat transfer.

5.2 TEST ASSEMBLY LAYOUT

The test assembly (TA) hybrid must accommodate the five modules as well as discrete electrical components. The TA layout approach is illustrated in Fig. 5-8. The placement of buffer/amplifiers and lead lines relative to the modules is indicated. The primary layout restrictions stem from the fact that each focal plane module is to be butted against at least one of its neighboring modules. This limits the available

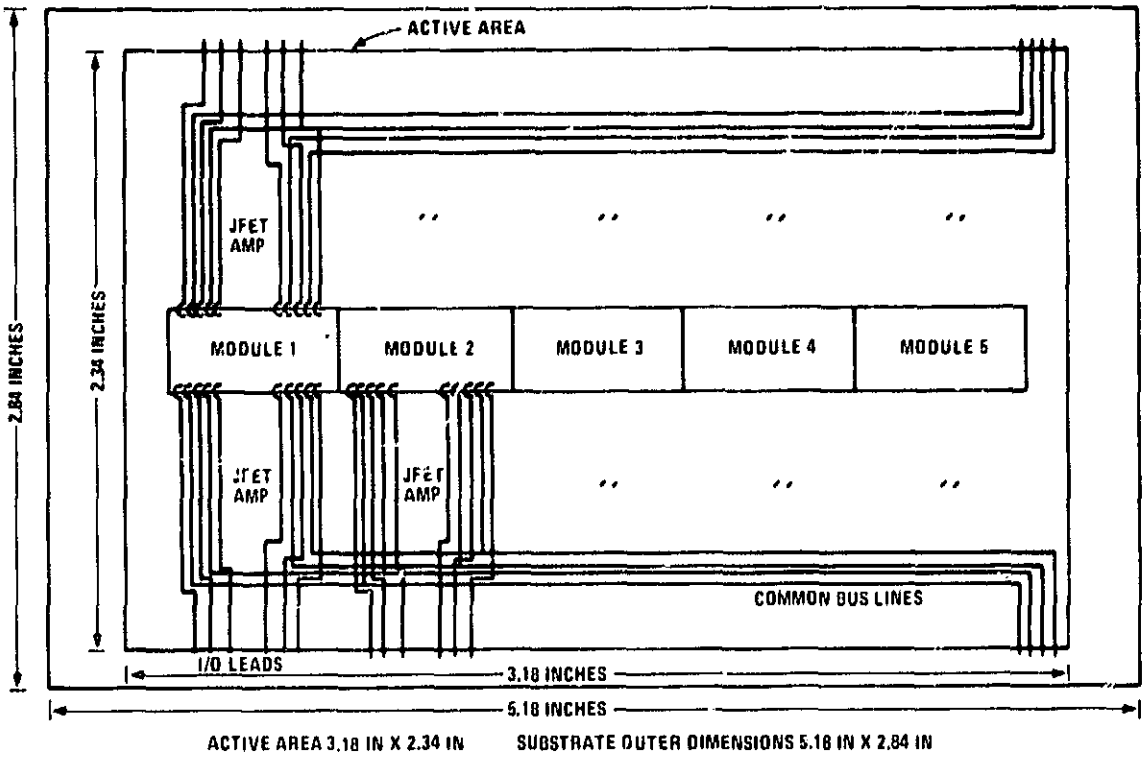


Fig. 5-8. Test assembly substrate layout.

linear dimension for the JFET buffer/amplifier and the fanout of the lead lines to that of the length of a module. In addition, the need for bypass capacitors, which are relatively large, also competes for available space. The utilization of 2-level metalization proved necessary to alleviate the space problem.

The test assembly is built around the five modules (600-x-150 mils), which are butted lengthwise to form a 3-inch-long focal plane. Each module contains two detector arrays with the pads emanating from the two opposite long sides.

The layout for a 12-module hybrid would be obtained by expanding the 5-module layout on the Applicon computer. The final 5-module layout would be stored in sections (cells) which correspond to the left edge, right edge, and center of the hybrid. Repeating the center cell five times will create the 5-module configuration. Repeating it twelve times would create the 12-module layout.

Studies conducted by Ball Aerospace during the MLA instrument definition study revealed that I/O connections result in considerable thermal leakage. For this reason and for the simplification of the edge connector, it is desirable to minimize the total number of leads on the hybrid. Without employing any lead reduction techniques, the total number of leads will be 240. Table 5-3 is a summary of the chip I/O functions and lead count for each.

Significant lead reduction can be accomplished by using common bus lines for certain clock and voltage supply lines. The total number of leads can be reduced to 184 by using common bus lines for the register clock phases ($\phi 2T$, $\phi 1T$, $\phi 1S$, $\phi 2S$), the input gates (G1A, G1B), and for the amplifier power supply (V_{D1}). In this case, 70 separate lines are reduced to 14 common bus lines. Additional lead

TABLE 5-3. SUMMARY OF CHIP I/O FUNCTIONS

I/O FUNCTIONS	Full Count (Repetitions x Leads)	Reduced Count (Repetitions x Leads)
CCD Register Clock Phases (ϕ_{1S}, ϕ_{2S}, ϕ_{1T}, ϕ_{2T})	10x4 = 40	2x4 = 8
CCD Input Gates (G1A, G1B)	10x2 = 20	2x2 = 4
CCD Input Gates (G2)	10x1 = 10	10x1 = 10
CCD Input Strobe (S1)	10x1 = 10	2x1 = 2
CCD Output Gates (ϕ_{DC1}, ϕ_{DC2}, ϕ_{RDC})	10x3 = 30	10x3 = 30
CCD Reset Gate (ϕ_{RG})	10x1 = 10	10x1 = 10
CCD Reset Drain (V_{DR})	10x1 = 10	2x1 = 2
Amplifier Supply (V_{D1})	10x1 = 10	2x1 = 2
Detector Transfer Gates (ϕ_{TR1}, ϕ_{TR2}, ϕ_{TR3})	10x3 = 30	10x3 = 30
Detector Shield (DET)	5x1 = 5	5x1 = 5
Substrate (Sub)	10x1 = 10	2x1 = 2
Temperature Sense Diode (Temp)	5x1 = 5	5x1 = 5
JFET Power Supplies (V_{S1}, V_{S2}, V_{S3})	10x3 = 30	2x3 = 6
Video Output (out)	10x1 = 10	10x1 = 10
Ground (Gnd)	10x1 = 10	2x1 = 2
TOTAL	240	128

reduction can be accomplished by using common bus lines for the reset drain (V_{DR}), the input strobe (S1) and the ground. Finally, if the voltage supplies (V_{D1}, V_{D2}, V_{D3}) and the ground for the JFET buffer/amplifier circuit incorporate common bus lines, the total number of leads is reduced to 128. Thus, a goal of the TA layout will be to attain a lead count of only 128.

5.2.1 Performance Requirements

Initially, 5-mil lines were considered due to the space limitations imposed by the module lengths. However, the large numbers of these lines would, in all probability, present a yield/reliability problem. By routing some of the lines through the JFET buffer/amplifier circuit via unused sections of its first-level metal, 10-mil lines and spacings were achieveable in subsequent hybrid layout designs.

A possible concern with using 5- or 10-mil common bus lines is that the added resistance may cause an unacceptable voltage drop. However, the following calculations show that this will not be a problem. First, the voltage drop for the highest current power supply line is calculated:

$R_S = 2\times10^{-3}$ ohm per square (resistance of 10-mil line)

$L_{max} = 3000$ mils (maximum bus line length, 5 module case)

$I_p = 2.5\times10^{-3}$ A (maximum power supply current)

$V_{max} = 15$ V (maximum power supply voltage)

$$R_{max} = \frac{2\times10^{-3}\ \text{ohm}}{10\ \text{mils}} \times 3000\ \text{mils} = 0.6\ \text{ohm}$$

$$V_{drop} = I_p R_{max} = 0.6\ \text{ohm} \times 5\times10^{-4}\ \text{A} = 1.5\ \text{mV}$$

or 0.01% voltage drop. Thus, there is not appreciable voltage drop on any of the DC lines. Next, the voltage drop for the register clock phases is calculated as follows:

$C = 250$ pF (capacitance per module-band for ϕ_{1T})

$\Delta V = 15$ V (maximum clock voltage difference)

$\Delta T = 200$ ns (rise time of clock pulse)

$$I_c = C\frac{dv}{dt} = C\frac{\Delta V}{\Delta T}\ \text{(maximum clock line current)}$$

$$I_c = \frac{(250\times10^{-12}\ \text{F})\ (5\ \text{modules})\ (\ 15\ \text{V})}{(200\times10^{-9}\ \text{s})} = 100\ \text{mA}$$

$$V_{drop} = I_c R_{max} = 100\times10^{-3}\ \text{A}\ (0.6\ \text{ohm}) = 60\ \text{mV}$$

or 0.4% voltage drop. Again, there is not appreciable voltage drop. Therefore, 10-mil line widths are acceptable with a wide margin.

5.2.2 First-Generation Layout

The hybrid layout should be designed to keep noise pickup to a minimum and should have the flexibility in its design to accommodate the possibility of future circuit modifications. A first-generation test assembly layout has been completed as part of the Design Trade Study. The layout is shown in Fig. 5-9.

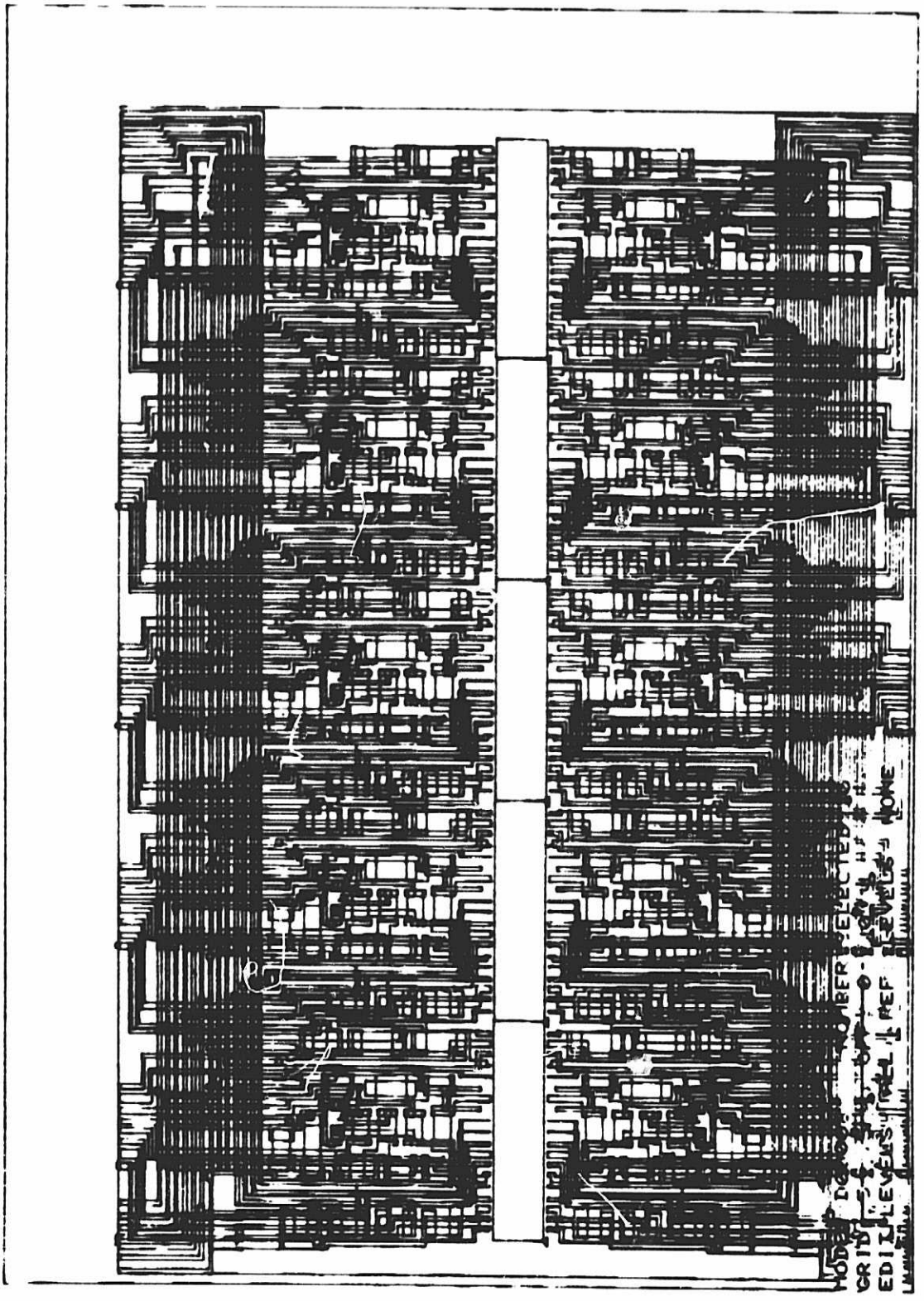


Fig. 5-9. First-generation test assembly layout.

The critical input/output associated lines (module output, JFET buffer output, G1B, G2, substrate and ϕ DC) were carefully routed to minimize clock line feed-through. This was accomplished by minimizing the area of crossover between the critical lines on one level of metalization and the clock lines on the other level. In addition, critical lines were routed in such a way as to avoid the situation of a neighboring parallel line being a clock line. For the case of the module output and the JFET output, the neighboring parallel lines were ground.

The JFET buffer was layed out in such a way to facilitate modifications of the original design. This was accomplished by the inclusion of additional nodes. During the buffer design refinement, a effort will be made to minimize the component requirement. The first-generation layout utilizes the current JFET buffer design. It is anticipated that the final buffer design will occupy a smaller area of the hybrid substrate than this first design.

The first-generation hybrid will contain numerous discrete components. Each JFET buffer currently contains three capacitors, four resistors, and two JFETs. For the 5-module (12) test assembly, there would be a minimum of 30 (74) capacitors and 40 (96) resistors. In addition to the JFET buffer components there will also be 12 bypass capacitors per module. For the 5-module (12) assembly this would result in 60 (144) additional capacitors. To reduce the total number of components some of the bypass capacitors may have to be omitted.

The 5-module assembly substrate outer dimension will be 5.18-x-2.84 inches with an active area (area hybrid actually occupies) of 3.18-x-2.34 inches. The 12-module test assembly dimensions would be 12.5-x-2.84 inches for the substrate with 7.63-x-2.34 inches of active area.

5.2.3 Test Hybrid Design

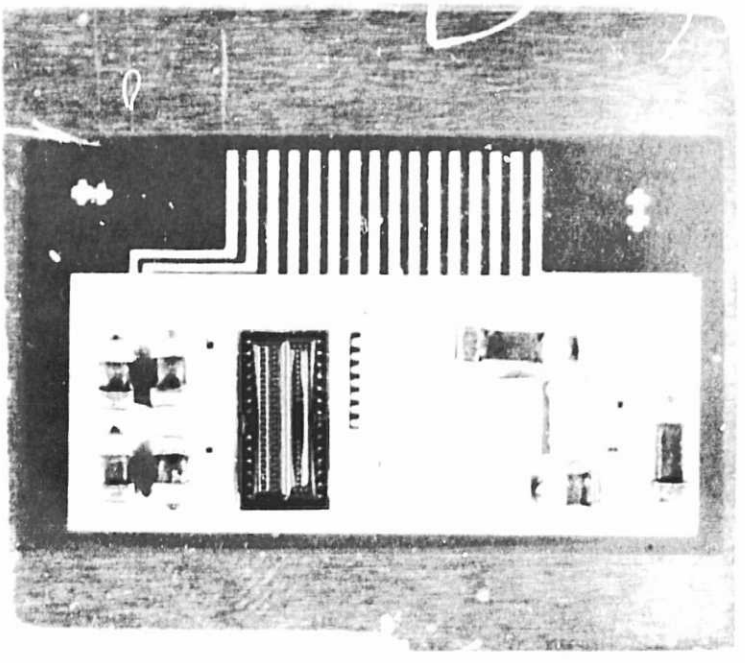
A test hybrid was designed and built. The hybrid circuit, shown in Fig. 5-10, has a high-density IRCCD test chip (TA11395) and a first-generation JFET buffer. The circuit will be utilized to evaluate the electrical characteristics of the buffer and the pickup characteristics of the hybrid technology. The buried-channel floating diffusion amplifier on the TA11395 is connected to the 2-stage JFET buffer. The circuit will be operated to evaluate the performance of the total output circuit (see schematic in Fig. 5-11).

The test hybrid will give valuable information on the printing characteristics of the thick-film materials. This test vehicle will also yield insight into optimum assembly techniques and the reliability of epoxy mounting.

This test hybrid effort will be followed by a detailed reliability assurance program for the thick-film-on-silicon technology. During this test program, large area test patterns will be utilized to access pin-hole defect density, epoxy bond yield, ball wire bond yield, and resistance to thermal stress.

5.2.4 Temperature Effects on Capacitance and Resistance

Because the testing and assembly of the hybrid will occur at room temperature while the expected operating temperature will be 100 to 125K, it was necessary to study the temperature characteristics of the individual hybrid components. Knowing



TEST FILM ON SILICON SUBSTRATE

Fig. 5-10. Test hybrid with JFET buffer.

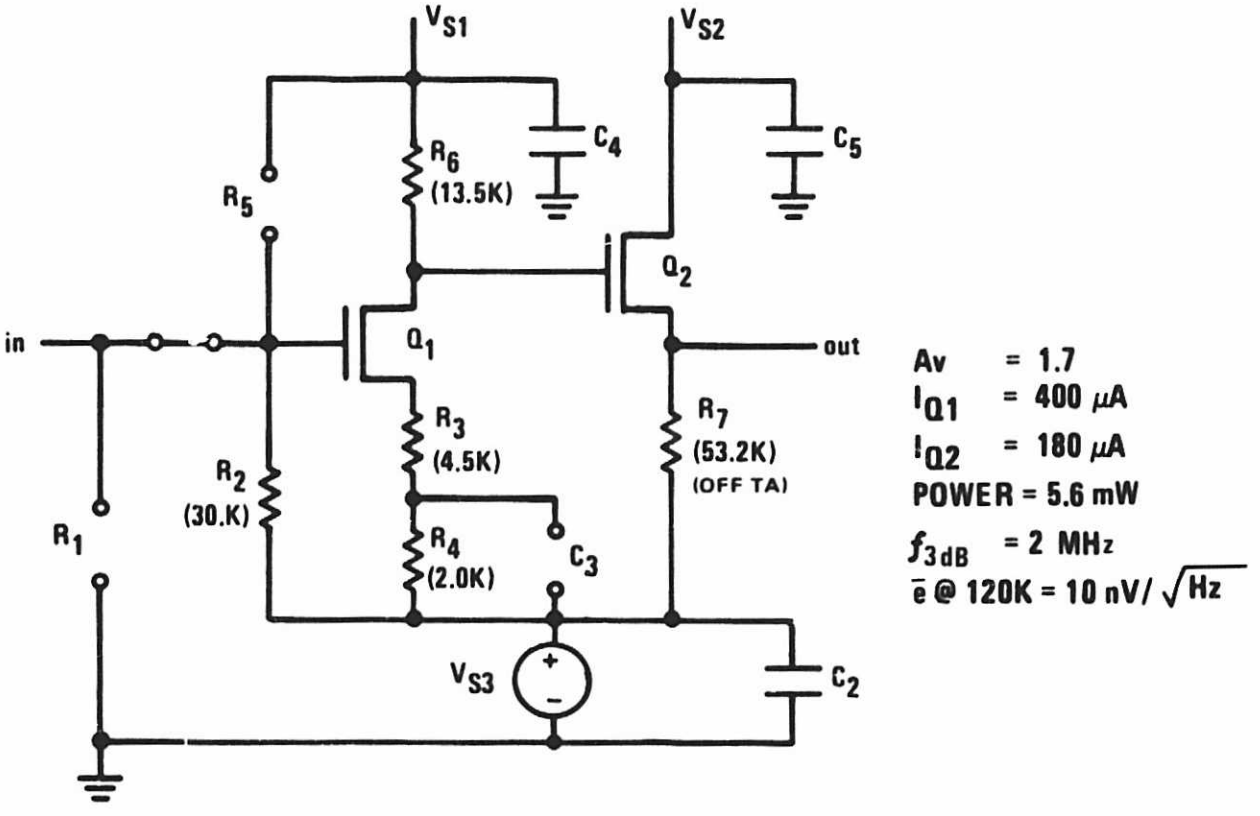


Fig. 5-11. JFET buffer schematic.

the parametric variation of component values due to temperature will enable room temperature values to be chosen such that their derated values at 100K will fall within design limits.

Sprague 194D capacitors were used on the test hybrid. The normal specification sheets supplied with these capacitors gave temperature characteristics for +125C down to only -55C. The temperature characteristics below -55C were obtained from a cyrogenic characterization study performed by the manufacturer. In the study, the capacitance was measured at 25C and -195C for different valued capacitors at different frequencies which ranged from 1 to 250 kHz. The combination of both sources of data were used to obtain a curve fit which shows the change in capacitance versus temperature over the needed range of temperature (Fig. 5-12).

Minisystems precision thick-film chip resistors were used on the test hybrid. As with the capacitors the manufacturer specification sheets supplied with the resistors gave temperature characteristics down to only -55C. However, our hybrid laboratory measured the change in resistance for these and several other types of resistors when the resistors were brought from room temperature to 77K by dipping in liquid nitrogen. A plot of the change in resistance versus temperature for three types of resistors is shown in Fig. 5-13.

The Sprague capacitors and Minisystems resistors will provide good performance at our cryogenic temperatures. We plan to utilize these devices for the test assembly. An evaluation of low-temperature JFET performance will be conducted during the second quarter of 1983.

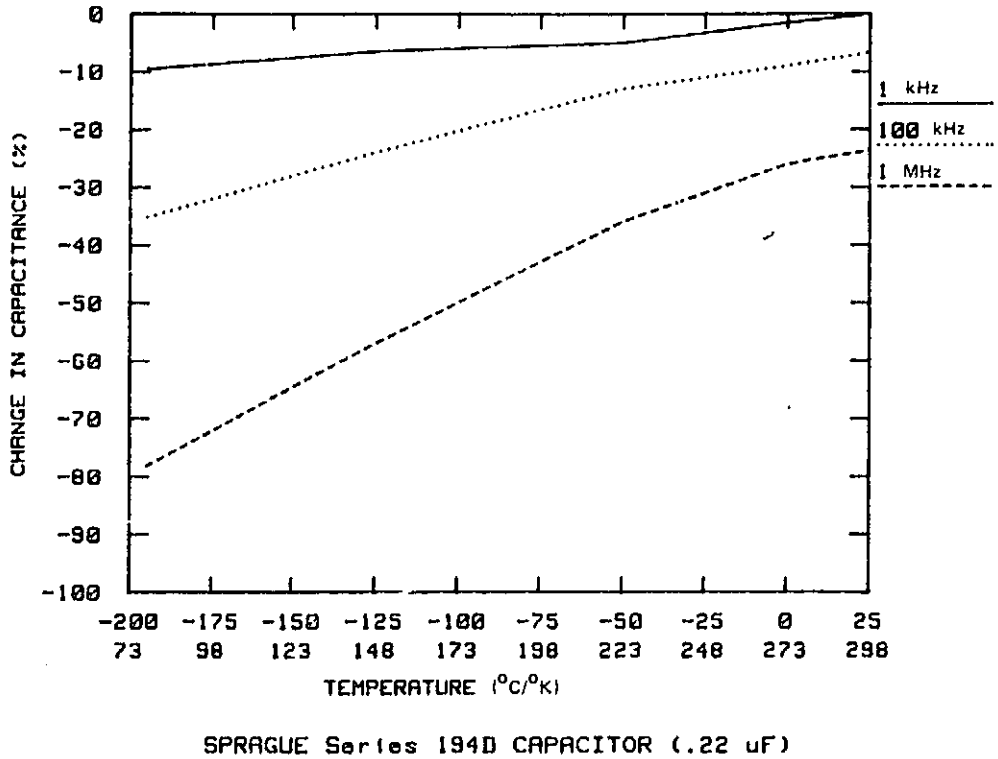


Fig. 5-12. Change in capacitance versus temperature.

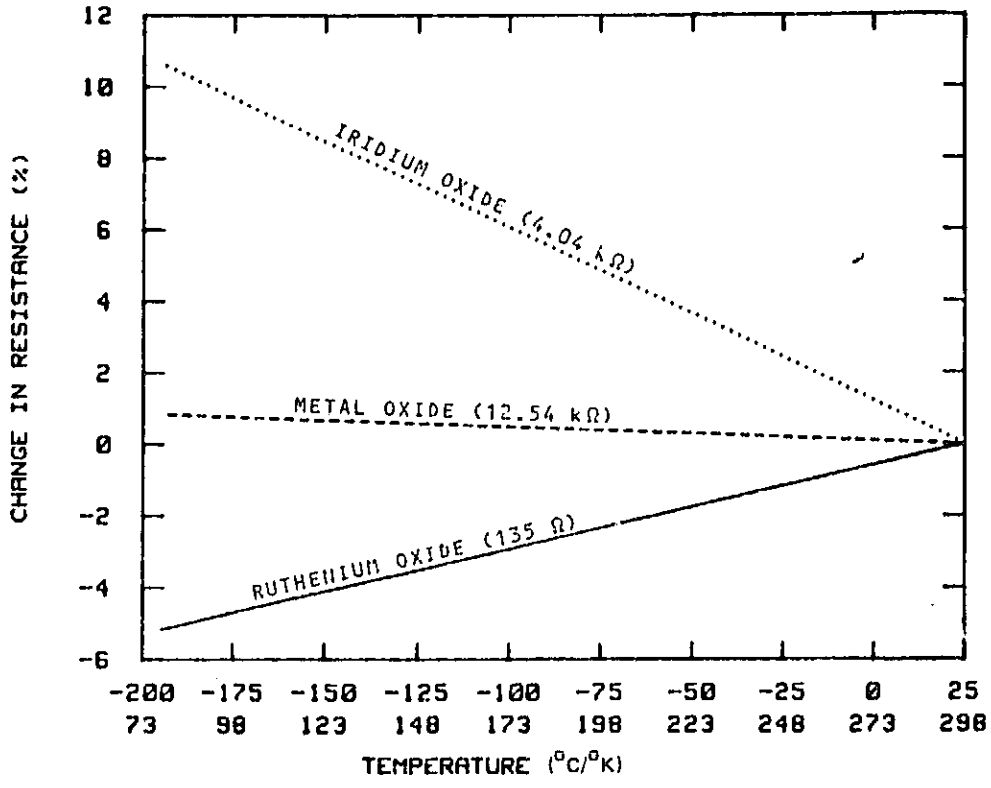


Fig. 5-13. Change in resistance versus temperature.

5.3 SYSTEM MECHANICAL AND THERMAL REQUIREMENTS ON TEST ASSEMBLY

This section* describes the requirements on the test assembly which are imposed by system considerations of a mechanical and thermal nature and suggests the features of the TA which are needed to meet these requirements.

5.3.1 Mechanical Requirements

It appears that most of the mechanical requirements on the TA are driven by the band-to-band registration requirements for the instrument. The allowed misregistration can apparently be as much as a few pixels since the need for resampling seems to have been accepted. However, the stability of the alignment needs to be very high during the period between redeterminations of the resampling coefficients. This period could be as long as one week.

There is also a severe requirement to preserve the focus of the instrument under launch loads and temperature cycling. The available depth of focus is only about 10 to 30 μm, depending on which version of the MLA is being considered. This need to preserve focus is more severe than the registration issue because resampling does nothing to improve focus. The focus adjustment made on the ground must, therefore, be maintained through launch and throughout the mission life, including temperature cycling. (This could be relaxed considerably if there were active focus control on the instrument, but neither BASD nor the other contractors have baselined this in any of their MLA designs.)

*This section was written by Ball Aerospace Division (BASD).

Considerations of these issues lead to the following requirements on the TA and the mounting and alignment scheme:

1. Alignable – The TA must be mounted in a fashion which allows position adjustment during installation in all three dimensions. (This assumes that the TA will not be perfect, i.e., that the positions of the detector elements with respect to the mounting reference surfaces of the TA will not be exactly the same for all of the TAs in the instrument.)

2. Predictable – The changes in position of the detector elements in all the TAs when the FPA is cooled to its operating temperature should be predictable to within about 30 μm, and should be repeatable to within about 0.1 pixel for different cooling cycles. This means that the alignment can be done warm, and that resampling coefficients do not have to be changed for each cooldown cycle.

3. Repeatable – This TA should be demountable and replaceable with reproducible precision. This precision should be less than 0.1 pixel or 3 μm, if possible, so that new resampling coefficients do not need to be determined after TA removal and replacement. (If new coefficients were not too costly then this repeatability could be relaxed to less than 50 μm or so.)

4. Stable – The positioning of the TAs with respect to each other in the focal plane assembly (FPA) must be stable to 0.1 pixel over a period on the order of a week, when the FPA is maintained at the operating temperature.

5. Launchable – The TAs must hold their relative alignment to within about 30 μm in the cross-track and down-track directions, and 10 μm in the focus direction, during the launch trauma. The FPAs might be either warm or cold during launch, depending on the MLA version.

6. Gentle – The mounting method cannot distort the TAs in any way which affects the registration or focus, other than that which is allowed as described previously.

5.3.2 Thermal Requirements

The thermal properties of the TA/instrument interface are determined by the temperature stability needs of the detectors, which are derived from the radiometric requirements for the instrument. In the BASD Instrument Definition Study the temperature stability requirements were derived using the theoretical dark current characteristics of the detectors. The radiometric requirements dictate that the detector dark current be stable enough to generate no more than about 0.25% radiometric error. This applies to the time between dark current calibrations. This means that the detector temperature must be maintained to about plus or minus 1K. Measurements on actual palladium-silicide detectors have verified the predicted dark current at the 120K operating temperature, so the conclusions in the BASD study appear valid. However, careful measurements around 120K to determine the slope of the dark current versus temperature are needed to fully verify theoretical performance.

In providing closed-loop control of temperature one should place the control sensor as close as possible to the control heater to facilitate the servo design and improve performance. This means controlling the temperature of the surface on which the TAs are placed, and making the thermal conductance from the detectors to the surface sufficiently small.

For the TAs which have been suggested this thermal conductance can be dominated by the conductance of the contact between the TA and the mounting surface of the FPA. The difficulty of making high-conductance cryogenic joints or contacts is well known (in cryogenic circles) and unless care is taken this contact conductance can be excessive. The power to be removed from the FPA for a full-up MLA instrument will be about 300 mW, including dissipation, radiation, and conduction through the wiring. This level will change somewhat depending on the signal level in the on-chip amplifiers, etc. This power change will create a temperature difference between the detectors and the temperature-controlled plate which is given by:

$$\Delta T \text{ (mK)} = R(\text{mK/mW})\, \Delta P \text{ (mW)}$$

where R is the thermal resistance in mK/mW and ΔP is the power fluctuation.

If we assume a R of 10 mK/mW and a total power fluctuation of 20%, the induced temperature change at the detectors is 600 mK. This is well below the 1K fluctuation limit, but we must leave some margin for the temperature control system.

These considerations lead to a single requirement on the TA and its mounting method, namely:

1. The thermal resistance between the detector chips and the mounting surface for the TAs should be less than about 5 mK/mW.

Again, since the resistance excluding the interface should be much less than this, the requirement boils down to the contact resistance only.

Since the control sensor should not be in the TA, the on-chip temperature sensing diodes will be used as monitors of the actual chip-to-FPA temperature difference, and of the chip-to-chip variations. These are valuable functions and the on-chip diodes should be maintained.

5.3.3 Preferred Approach

The mechanical alignment and stability requirements previously listed are stringent, while the thermal requirement is, relatively speaking, more straightforward. The design approach is therefore to determine a TA and mounting method which satisfies the mechanical needs, then choose a thermal interface method which is consistent with it.

5.3.3.1 TA Mounting and Alignment

The mounting and alignment method which offers the most flexibility is to position the TAs on the FPA using spring-loading against shimmed tabs which contact the edges of the TA. This is shown in Fig. 5-14.

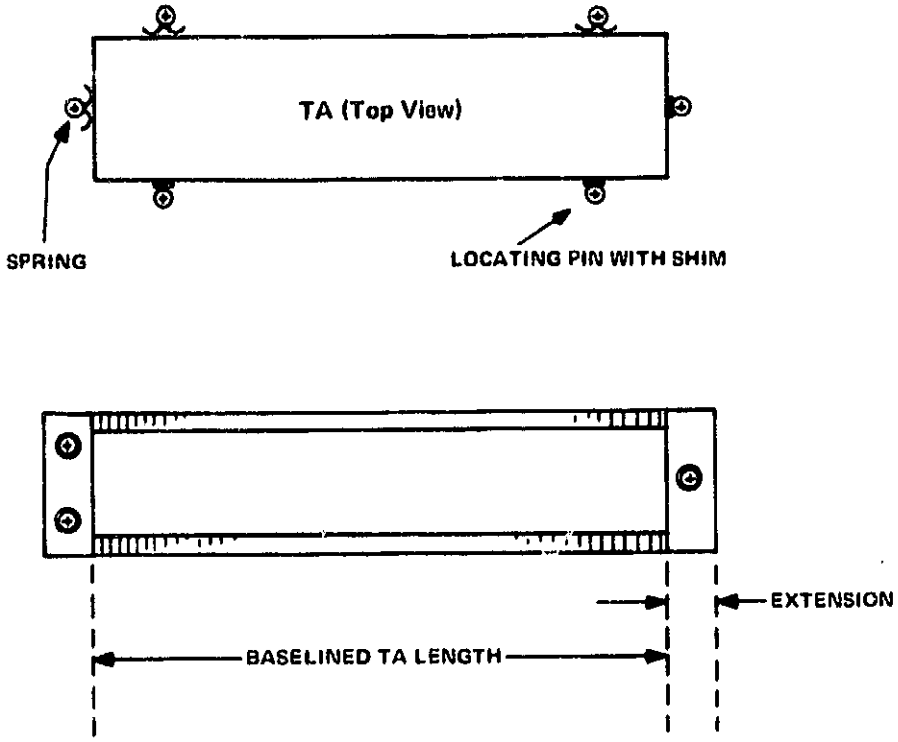


Fig. 5-14. Mounting and alignment.

Because the edges of the TA serve as the reference for the registration procedure, they should be square both to each other and to the bottom surface, and also have a good quality finish. When the TA is measured, the detector positions should be reported with respect to the edges to be shimmed in the FPA.

The holddown would most likely be screws or clamps with belleville-like washers. The proposed TA concept should be slightly modified by adding some length to allow clearance holes for holddown screws, or for clamping surfaces, as also shown in Fig. 5-14.

5.3.3.2 Thermal Contact

Achieving the required thermal resistance, less than 5 mK/mW, requires care and experience. A thermal resistance of 1 mK/mW at 120K is very respectable. For example, a bolted aluminum-to-aluminum joint under moderate pressure can easily exceed 10 mK/mW. Dielectric-to-metal joints require a certain amount of caution and care. A sapphire-to-copper joint can show a disastrously high resistance, which is improved 10,000 times by the inclusion of a thinfoil or film of gold at the interface. Yet, gold plating an aluminum joint can increase the thermal resistance 100 times at 4K.

One approach to reach the required amount of thermal contact between the TA and the FPA is a simple mechanical clampdown. Experts (at BASD) in the fabrication of cryogenic joints have recommended a gold plating on the mating surface of the TA. This is particularly advisable since the TA surface is a semiconductor. If some care is used in the design and material selection of the mating surface in the FPA, there should be no problem meeting the required 5 mK/mW.

5.3.4 Derived TA Requirements

From the considerations just presented we conclude that even without detailed design of the FPA, the requirements on the TA which relate to mounting, alignment, and thermal interface to the FPA can be defined. These requirements are:

1. The silicon plate which provides the mounting surface of the TA should be accurately square, with flat and smooth faces. This helps to achieve reliable and repeatable positioning.

2. The TA package should be extended in length and provided with clearance holes for holddown screws with belleville washers.

3. The mounting surface of the TA should be optically flat and provided with a gold coating to facilitate thermal contact to the FPA, regardless of the contact method used.

5.4 TEST ASSEMBLY LEADS

This section* outlines the thermal loads imposed on the focal plane cooler by the leads to the focal plane, and provides information to aid in the design tradeoffs involved in the choice of the number and type of leads.

5.4.1 Results From the Instrument Definition Study

The BASD MLA Instrument Definition Study included the design and modeling of both radiative and stored cryogen coolers for achieving the 120K operating temperature for the SWIR focal plane. The following sections summarize the study results.

5.4.1.1 Leads Baselined in the Study

Since it was not known in advance what type of leads would be required, the modeled lead configuration reflects the conservatism common to that stage of the design effort. We assumed that, as a worst case, coaxial leads might be required to keep crosstalk and other pickup to sufficiently low levels. This is a worst case thermally, but also presents some electrical problems since a coax presents a large load to a low-power on-chip CCD output stage.

The leads actually used in the modeling effort were the stainless steel coaxes used in the IRAS program, for which the thermal data were readily available. The following list gives the electrical and thermal data for the wire:

1. Conductors: Stainless steel

2. Dielectric: Teflon

3. Electrical Impedance: 40 ohms at 10 MHz

4. Electrical Resistance: 12 ohms per foot

*This section was written by Ball Aerospace Division (BASD).

5. Capacitance: 25 pF per foot

6. Thermal Conductance (200K to 120K, 1-foot length): 0.21 mW/K

5.4.1.2 Lead Configuration and Number

The number of leads baselined in the study was a total of 90 for the SWIR focal plane, all of which were baselined to be coaxial. The functions of these wires are given in the BASD and RCA study reports. Some functions were supplied in parallel to all chips, while some were supplied with a separate lead to each chip, depending on the nature of the function. This lead count is therefore a reasonable first cut based on a careful evaluation of the nature of each lead function.

In the study we assumed that the focal plane signal output would be sent to preamp/linedrivers located one foot away at an intermediate temperature heat station. The other leads were to be thermally tied to this station. All lead lengths were therefore one foot between the focal plane and this heat station at about 200K. We still believe that this configuration is appropriate. The drive capabilities of the focal plane modules designed by RCA are consistent with this.

5.4.1.3 Cooler Heat Loading for the MLA Instrument

The modeling of the MLA radiative cooler gave the following thermal load budget for operation at 120K:

1. Detector dissipation: 240 mW

2. Orbital flux: 100mW

3. Instrument flux: 80 mW

4. Lead conduction: 20 mW

5. Other conduction: 40 mW

6. Heater (control): 520 mW

7. Total: 1000 mW

The thermal loading from the leads, 20 mW, is negligible, even for this worst-case baseline.

5.4.2 Conclusions

The preceding discussion leads to these conclusions:

1. Heat load to the SWIR cooler from the leads should not be a major portion of the total heat load.

2. This allows flexibility in the type of lead used, the number of leads used, and the length of the leads. This will allow maximizing the electrical and radiometric performance of the focal plane without compromising thermal performance.

3. Testing of the SWIR test assemblies should be used to establish what type of leads are needed to meet the performance objectives.

5.5 FILTER IMPACT ON SWIR FOCAL PLANE ASSEMBLY

This section* describes the requirements made on the SWIR focal plane assembly by stripe filters. The driver is the separation between the ground tracks for the bands and should be determined by considerations related to data quality and processing needs. The separation currently allowed is assumed to be 10 IFOV, which is the limit stated in the SWIR SOW.

5.5.1 MLA Spectral Separation and Registration

The goal of the MLA program is perfect registration. To achieve this the line arrays for each band would have to be physically superimposed which at this time is impossible to do. Several options which approach the goal to varying degrees involve physically separating the detector arrays for the bands. The options which have been suggested so far are:

1. Optical superpositon (using beamsplitters)

2. Closely spaced line arrays with stripe filters

3. Spectral dispersion onto closely separated arrays.

The first option offers perfect registration in principle. There are optical and spectral limitations, but this method can be made to work.

The second option is obviously not registered, but if the spacing between the arrays is sufficiently small then performance is not compromised. The relative alignment between the arrays is perfectly maintained. Problems here are that for sufficiently small spacing it is difficult to build the detector arrays and especially the filters. This discussion will explore the extent of this difficulty.

The third option is the most elegant and powerful in principle. There are no filters to worry about but the burden is foisted onto the optics. This is the only system put forth to date which can have ground selection of the spectral bands over an attractively wide range, all done electronically at the focal plane. The focal plane is much more complex, using area arrays, and the registration is only as perfect as the distortion in the spectrometer will allow.

Note that the first two options can be combined if desired. For example, the SWIR could be split off (Option 1) to be a focal plane with stripe filters over closely spaced arrays (Option 2).

In directing RCA to build development focal planes in both the SWIR and the VIS/NIR, Goddard has indicated that a preliminary decision has been made to proceed with a system approach that uses the second option. However, the SWIR SOW does not require the inclusion of filters in the package, or even that the focal plane package be consistent with producible stripe filters. Of late this oversight has been

*This section was written by Ball Aerospace Division (BASD).

recognized and RCA has been directed to consider the filters and, if possible, to produce a focal plane package which is filterable. There is still no requirement to supply filters with the deliverables.

The important constraints placed on the detector array and the focal plane package by the stripe filters have been derived. The key ingredient in this is the allowed separation between the two (or more) detector line arrays, usually expressed in units of IFOV. In our (BASD) original look at this problem in the system definition study, we allowed ourselves only three IFOV center-to-center spacing. This was mandated by our perception of the registration requirements. At that spacing it is extremely difficult to produce the stripe filters, because the separation between the filters is too small (according to OCL1). It is apparent, however, that Goddard believes that a spacing of 20 IFOV is acceptable. This is shown by the SOWs for the RCA development contracts and by statements from Goddard personnel. At these spacings the filters are at least possible, and this supplies the motivation for this more detailed look at the requirements.

5.5.2 Filter and Detector Model

The model used to describe the filter and detector is given in Fig. 5-15. The detector array is assumed to be backside illuminated. The surfaces, thicknesses, and indeces of refraction of the media are labeled with subscripts as shown. The pitch of the detector array is assumed to be 30 μm. The half-angle of the converging light is assumed to be that of an f/4 optical system (i.e., 7.1°). Medium 2 is a substrate for filters.

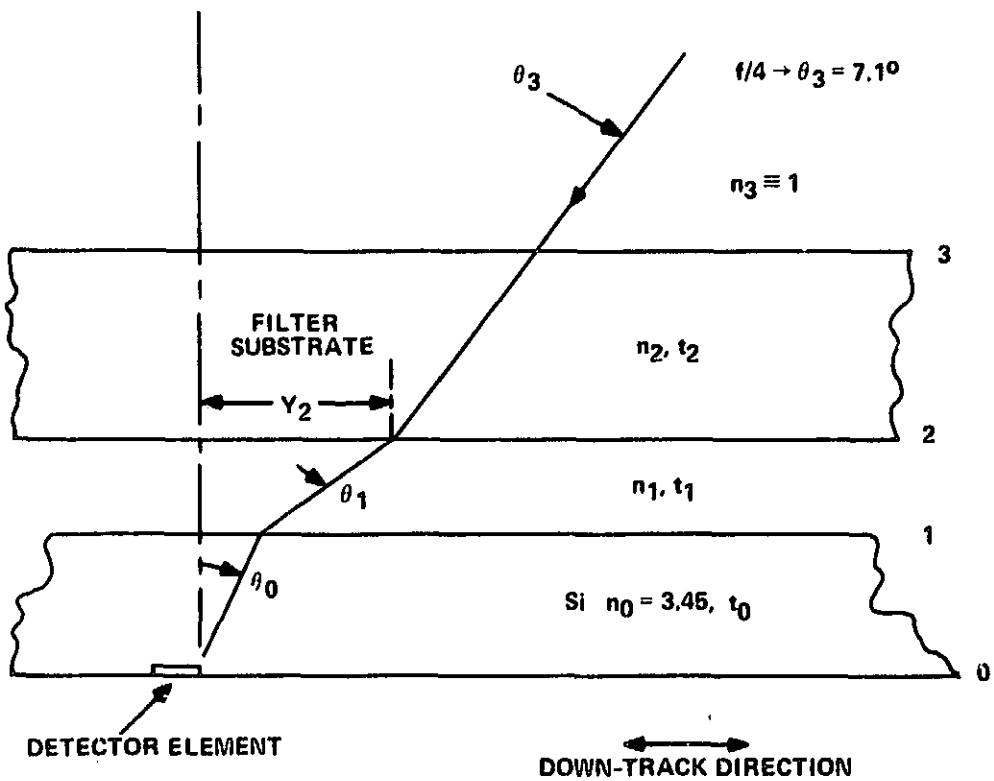
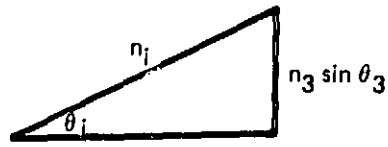


Fig. 5-15. Filter and detector model.

From Snell's law we have

$$\sin\theta_i = \frac{n_3}{n_i} \sin\theta_3$$



The beam width:

$$y_N = \sum_{i=0}^{N-1} t_i \tan\theta_i$$

$$= \sum_{i=0}^{N-1} t_i \frac{n_3 \sin\theta_3}{\sqrt{n_i^2 - n_3^2 \sin^2\theta_3}}$$

$$= n_3 \sin\theta_3 \sum_{i=0}^{N-1} \frac{t_i}{n_i} \left[1 + 1/2 \left(\frac{n_3}{n_i}\sin\theta_3\right)^2 + \ldots\right]$$

$$y_N = n_3 \sin\theta_3 \sum_{i=0}^{N-1} \frac{t_i}{n_i}$$

where n is the index of refraction, t is the thickness, and y is the half-width of the light beam from the optics for a line at infinity.

For the bands to be spectrally separated the center-to-center spacing of the detector arrays must be

$$C_N = (2y_N + p + g)/p \quad \text{(pixels)}$$

where p is the element size in the down-track direction, and g is the space separating the good parts of the filter stripes in the down-track direction. As g gets bigger the filters become easier to make. Present evidence suggests a g of 100 μm makes filter fabrication possible but not easy.

Medium 0 will of course be silicon. Its thickness can be in the range from 250 to 500 μm without any strain. (This is the range of commercially supplied wafer thicknesses. Thinner wafers are very difficult to handle for one reason or another). The index of silicon in the SWIR is about 3.45. Note that in the expression for y the contribution from each layer is proportional to the thickness divided by its index. This means that air gaps and glass between the filter and the detector will be much more painful than the same thickness of detector substrate.

5.5.3 Results

The most probable configuration will be with filters on surface 2. (For filters on surface 1 the chip yield will most likely be far too low.) For the following values:

p = 30 μm

g = 100 μm

we have

$$C_2 \doteq \frac{t_0}{420} + \frac{t_1}{120} + 4.3 \quad (t \text{ in } \mu m)$$

where C is given in units of IFOV (30 μm at the detector). For t_0 = 300 μm (12 mils):

$$C_2 \doteq 0.7 + \frac{t_1}{120} + 4.3$$

where t_1 is in μm and C in IFOV.

The portion from the silicon detector substrate is almost negligible compared to the overhead imposed by the filters (g). To make the packaging reasonable, and to permit a package with removable and interchangeable filters if possible, we would like t_1, the air gap, to be large. But an air gap of only 600 μm (24 mils) takes up the maximum allowed 10-IFOV separation between the detector line arrays. This is not very comfortable for a package with removable filters, but it would allow room for mounting nonremovable filters using several approaches.

The very high index of silicon suggests that air gaps are to be avoided, and that it may be feasible to get a larger effective gap for mounting purposes by filling the gap in the light path with silicon, as shown in Fig. 5-16. There are several ways this might be done. This will be explored in the report to follow on packaging.

5.5.4 Conclusion

Relaxing the band-to-band separation on the focal plane to 10 IFOV allows filter-to-filter and filter-to-detector spacings which are tight but would probably permit a package to be built which is consistent with RCA's current approach.

5.6 MLA MULTISTRIPE FILTER PACKAGING

This section* summarizes methods to include optical filters in a MLA-type instrument in the SWIR focal plane assembly. The main difficulty lies in the multi-band or multistripe nature of the focal planes which NASA requests, especially if changing filter bandpasses in flight is needed.

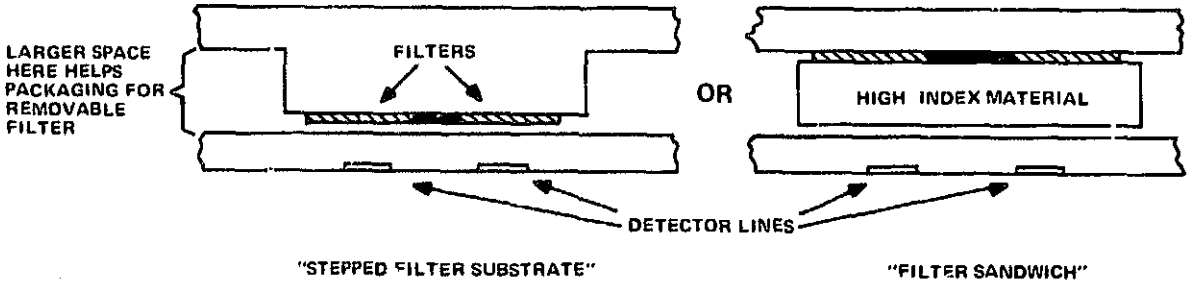


Fig. 5-16. Filter configuration.

*This section was written by Ball Aerospace Division.

5.6.1 Review Of Requirements

As noted in the previous section the motivation for interchangeable filters is strong to remain competitive with an imaging spectrometer approach. The conclusions of the previous section were that:

1. For an allowed stripe-to-stripe spacing of 10 IFOV on a multistripe focal plane, the filter must be within 500 μm of a backside illuminated detector chip. This applies only for an air (or vacuum) gap between the filter and the detector chip.

2. For a different medium in the gap, the gap can be increased by a factor equal to the index of refraction of the medium. For example, if the medium in the gap were silicon (index of 3.45), then the gap between the filter and the detector chip must be less than about 1700 μm.

Another requirement which should be kept in mind is that the positioning of the active volume of the detectors along the optical axis needs to be quite precise and stable. The MTF budget for the MLA-type instruments allows only about 20 to 40 μm tolerance at best, to be divided among all the structures which position the detector elements with respect to the telescope. It will almost certainly be necessary to fine tune the position of each detector package after assembly of the instrument. This means that the mechanical path from the detector elements to the reference mounting surface must at least be very stable. All the package configurations considered here are similar in this respect.

5.6.2 Proposed Focal Plane Packages

Two different packages have been suggested for the MLA-type focal planes with multistripe detectors and backside illuminated detector chips — one by RCA and one by BASD. The principal difference is the ease with which filters can be included.

5.6.2.1 Proposed RCA Focal Plane Package

RCA's detector package is shown in Fig. 5-17. Note that multiband filters would have to be positioned at the bottom of the deep (6 mm) stepped recess which admits light to the package. The advantage of this packaging method is that the butting of the detector chips can be done directly on the flat surface of the package, and is therefore simpler than that for the BASD study package.

5.6.2.2 BASD Study Suggestion

The BASD package scheme is shown in Fig. 5-18. This method would use "bump-bonding" to deal with back-illuminated detector chips. This method of interfacing back-illuminated CCDs is commonly used in the IR hybrid array business and is well proven and reliable. In this approach the physical mounting of the chips is through the electrically active side, leaving the backside (the optical input side) free of packaging incumbrances. Potentially this offers more flexibility for the inclusion of multiband filters.

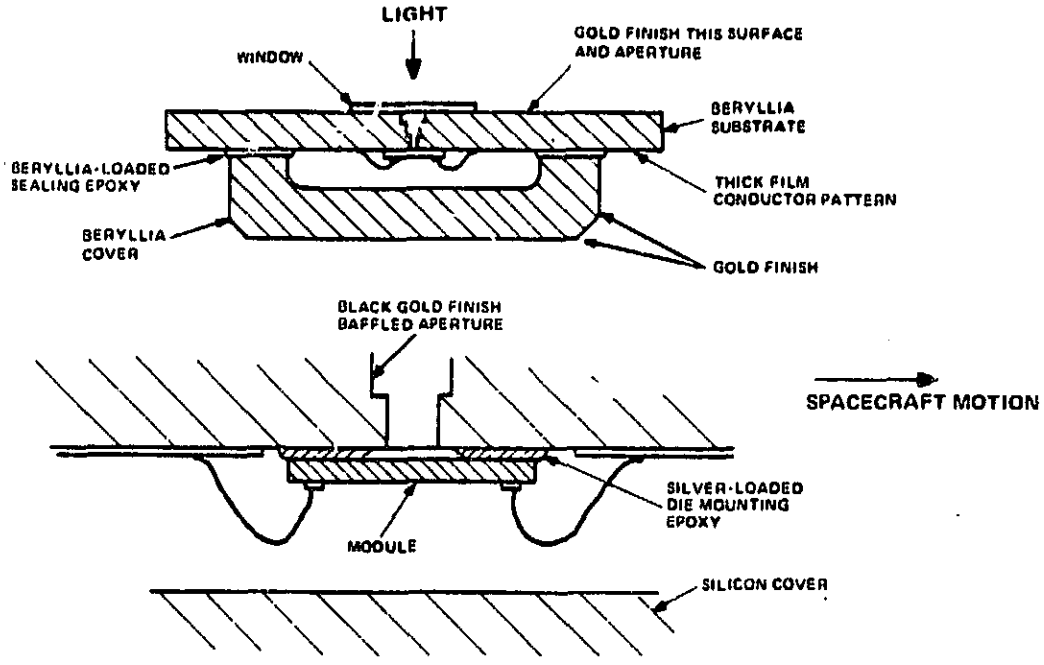


Fig. 5-17. Focal plane package.

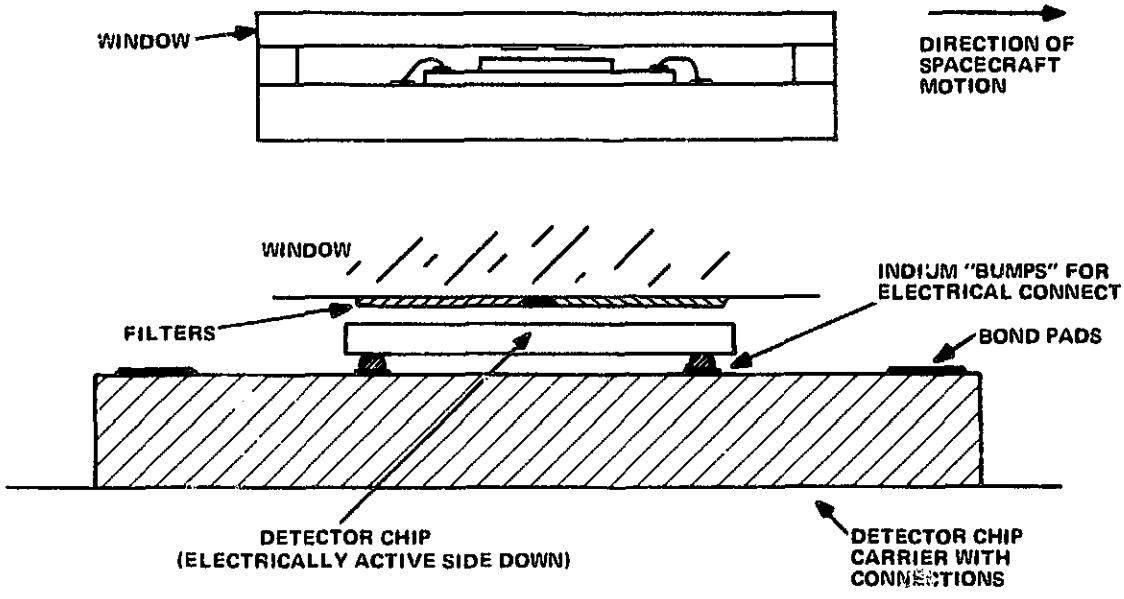


Fig. 5-18. Bump-bonding packaging.

A disadvantage is that the detector chips have to be "bump-bonded" to a carrier which then has to be attached to the mounting surface in the butting process, adding an extra fabrication step. Rockwell is experienced with the bump-bonding technique and claims that when indium bump-bonding was first proposed they were worried about the reliability, but their experience has been that it is simple and is the most reliable step in the whole process of making hybrid arrays for operation at cryogenic temperatures.

5.6.3 Some Approaches to Filter Packaging – RCA Baseline

5.6.3.1 Filters on the Detector Chips

This method positions the filters as close as possible. As shown in the previous section, the detector chip can be the standard thickness of 250 to 500 μm, or even more if desired. This approach was rejected because the yield multiplication for the filters and the detectors would make the filter/detector yield prohibitively low. This option is also not very exciting for interchangeable filters, unless the entire detector/filter package is exchanged.

5.6.3.2 Filters (Modules) on Glass Glued to Detector Chips

Each module would consist of a detector chip glued to a filter "chip" of the same size. When the modules are butted together, the glass filter substrates are also butted together causing some vignetting and crosstalk at the glass-to-glass interface, as shown in Fig. 5-19a. However, this approach allows no interchangeability of filters.

5.6.3.3 One Long Filter With Chips Glued in Place

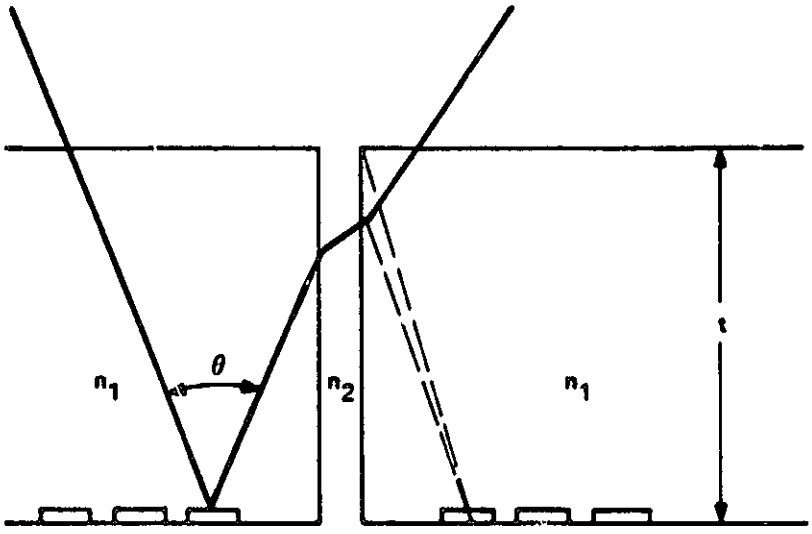
This method is very similar to the previous one except that the filter is one piece. This raises yield questions which are difficult to evaluate. Also, one long filter is harder to fabricate than short segments, but there is no vignetting as in the previous method. Again, there can be no filter interchange without replacing the whole package.

5.6.3.4 Filter Attached to the Package

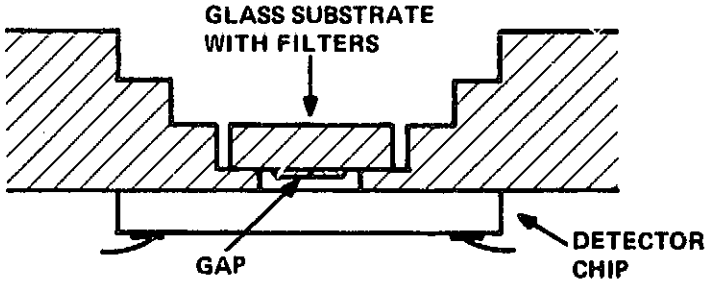
In this approach the filter (presumably one long substrate) is attached to one surface of the package (see Fig. 5-19b). The filter needs to go at the bottom of the recess in the RCA package. It could go on either side, but there seems to be no advantage to putting it on the inside. In the RCA package this approach presents some difficult machining problems. This gap between the filter and the detector chip can be no more than 500 μm if air spaced and no more than 1.7 mm if silicon spaced. The RCA package is baselined to be silicon and the thickness of the plate on which this mounting will occur is baselined to be 6 mm thick.

Since silicon is quite transparent at the SWIR wavelengths, the plate does not have to be machined completely through as shown in Fig. 5-19c. The surfaces in the optical path would have to be well polished and perhaps antireflection coated. It would allow one to use the maximum allowable gap of 1.7 mm.

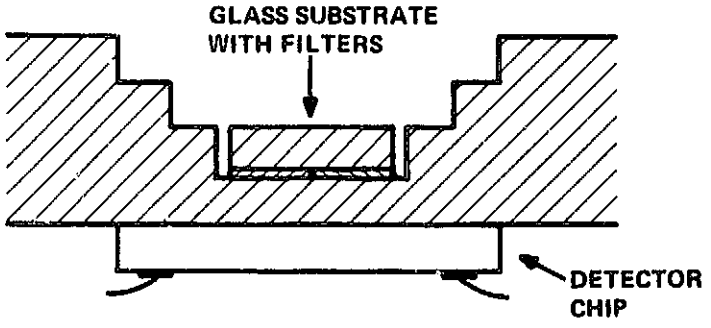
For ground interchangeable filters there would need to be some type of non-permanent alignment and attachment material at the bottom of the recess. For the goal of flight interchangeability this approach appears hopeless.



a. Detector chip glued to a filter of equal size.



b. Attached filter showing gap between it and detector chip.



c. Attached filter showing no gap between it and detector chip.

Fig. 5-19. Filter packaging approaches.

5.6.4 Filter Packaging – BASD Study Baseline

The major difference from the RCA package is that the optical input side of the detector chips (the "backside") is accessible, since the mounting surface is not in the way. In principle at least, this makes filter placement much simpler.

With this approach the package can be left open, giving direct access to the optical-input side of the detector chips. This is perhaps the only way to even approach flight interchangeability of filters with multiband or multistripe focal plane packages. Leaving the package open is, however, not desirable, especially in the SWIR which is cooled to cryogenic temperatures and is in an evacuated enclosure. The filter manipulating mechanism would have to be in the vacuum cryostat enclosure.

5.6.4.1 Filters on the Window

This is the approach suggested by BASD in the Instrument Definition Study Report. At that time it appeared to be the most viable approach from the point-of-view of filter implementation. The package is shown in Fig. 5-19b. The key feature is that the filter substrate (window) is not used to mount the detector chips. The window serves only to seal the package and carry the filters on its inside surface, which is ideally situated to this job.

For non-interchangeable filters the window would be permanently sealed. To achieve ground interchangeability the window attachment could be nonpermanent (e.g., low-temperature solder or elastomer gasket). For a nonhermetic or vented package the window could be clipped on in some mechanically stable way.

5.6.4.2 Filter/Detector Module

This would use filter/detector modules similar to those discussed in Section 5.6.3.2. There would be no advantage in using the bump-bonding approach over the RCA baseline package. The filters would not be interchangeable.

5.6.4.3 No Window – Open Package

This one is mentioned only for the sake of completeness. Without a window there would be free access to the detector chip, and it would be possible to swing different filters in and out and place them close to the detectors with some skyhook which, for the SWIR, is in the cryostat enclosure.

5.6.5 Spectral Flexibility Without Filter Interchange

An instrument approach having spectral flexibility approaching that of an imaging spectrometer is under study now at BASD. This approach would use a beamsplitter to divide the telescope beam into broad spectral ranges. These outputs would fall on focal plane assemblies with fixed multistripe filters. For example, four beamsplitter outputs each with a four-stripe filter/detector package would give 16 possible spectral bands. Band selection would be done electronically and determining which bands to telemeter would be commandable from the ground.

This approach appears to be much simpler, to have less risk, and to be less expensive than the imaging spectrometer approach. It could easily be built in an inexpensive prototype MLA mode for proof of concept. For example, one might have no beamsplitter and one filter/detector assembly, with selection among the four possible bands by ground or shuttle command. This concept is continuously expandable up to any desired number of spectral bands.

5.6.6 Conclusions

It appears that the only conceivable way to combine a multistripe focal plane with flight interchangeable filters is with an open focal plane assembly, i.e., one in which the detector chips are exposed to allow some mechanism to swing filters out and in to within the necessary spacing limit. This approach might be implemented for the VIS/NIR focal plane, but for the evacuated SWIR focal plane at cryogenic temperature it seems out of the question.

Ground interchange of the multistripe filters is much easier (and cheaper) than flight interchange and can probably be implemented with either the RCA baseline package or the BASD study baseline. Of these two the BASD package seems to be much easier to implement because the optical input side of the detector chips are not used in the mounting of the chips.

Noninterchangeable multistripe filters can probably be done with either package approach. The easiest method seems to be with the BASD package having filters on the inside of the window.

Interchanging filters might be most easily done by changing the entire detector assembly with filters included, since to do the ground interchange the assemblies would have to be removed anyway. This would of course require an assembly for each filter combination desired, making this option relatively expensive.

Doing away with stripe filters would make the goal of mechanical flight interchange easiest to achieve. In this approach each detector assembly would be used for only one band at a time. Since the filters do not have to be extremely close to the detector chips, there would be many more options for their location and the tolerances would be much relaxed. This approach would not fully utilize the dual-stripe chips which RCA is currently planning. They might be used to give redundancy however. The instrument for such an approach would employ beamsplitters as proposed by BASD and others in the Instrument Definition Study.

Mechanical interchange of filters in flight does not appear to be a sensible approach to spectral flexibility for the MLA instrument. Electronic selection of spectral bandpasses for telemetry is much superior. This can be readily done with multistripe focal plane assemblies such as those being developed by RCA, perhaps with equal flexibility and much less expense than an imaging spectrometer.

Section 6

BENCH TEST AND CALIBRATION EQUIPMENT

6.1 TEST ELECTRONICS OVERVIEW

A preliminary test electronics block diagram is shown in Fig. 6-1. The important feature in the block diagram is the use of optical couplers between the TTL electronics and CCD electronics. The intention is to isolate the +5-V power supply and TTL logic completely from the analog electronics. At the outside of the CCD cold chamber will be a correlated double sampler (CDS) preamplifier. The preamplifier's purpose is two-fold. First, it will minimize the pickup that the signal encounters due to appreciable lead length at relatively high impedance. Secondly, it will have a very low output impedance which will have the capability of driving a 2-foot coax with minimum pickup. To maintain the benefits of minimized pickup care will be taken in establishing the grounds of the data acquisition system and the CDS circuitry.

The power conditioning utilizes double regulation for the driver, bias, and CDS boards. The timing and control board will have its own +5-V supply to reduce analog signal contamination from TTL switching circuits. Figure 6-2 illustrates the system power conditioning.

6.2 TIMING AND CONTROL

The basic philosophy incorporated in the design of the timing and control circuitry was one that would give the test engineer a degree of flexibility in exercising the various functions and evaluating the line sensor.

To operate the sensor array, nine timing pulses are essential. They are ϕ_{1T}, ϕ_{2T}, ϕ_{1S}, ϕ_{2S}, ϕ_{RG}, ϕ_{S1}, ϕ_{TR1}, ϕ_{TR2}, and ϕ_{TR3}.

The first four of these are required for CCD clocking. Pulse ϕ_{RG} resets the output floating diffusion after each pixel is read out. Pulse ϕ_{S1} strobes an electrical "word" (ϕ_{WD}) at the input of the CCD register, and ϕ_{TR} (ϕ_{TR1}, ϕ_{TR2}, ϕ_{TR3}) "dumps" the 512-pixel infrared signature into the CCD for serial readout.

Three other timing waveforms are needed for overall system operation. The previously mentioned ϕ_{WD} is inputted to the CCD and serially clocked through the 512-stage register and readout. It is used in evaluating the CCD transfer inefficiency. The timing and control board will contain a 5-pole switch so that ϕ_{WD} can be chosen from five different pulse rates. The last two pulses, ϕ_{CLP} and ϕ_{SM}, will be used on the CDS board and are essential in performing the CDS function.

Some flexibility has been built into the location of ϕ_{RG}, ϕ_{S1}, ϕ_{TR}. These pulses, through switch selection, can be placed anywhere in one CCD clock cycle and have arbitrary width. These can be seen as the dashed waveforms in Fig. 6-3. In addition, ϕ_{TR} can be set for integration times equal to 512 times the CCD clock period, 1024 times the clock period, and 2048 times the clock period. For evaluation of the imager at multiples of the nominal integration period this corresponds to integration times of 1.8 ms, 3.6 ms, or 7.2 ms.

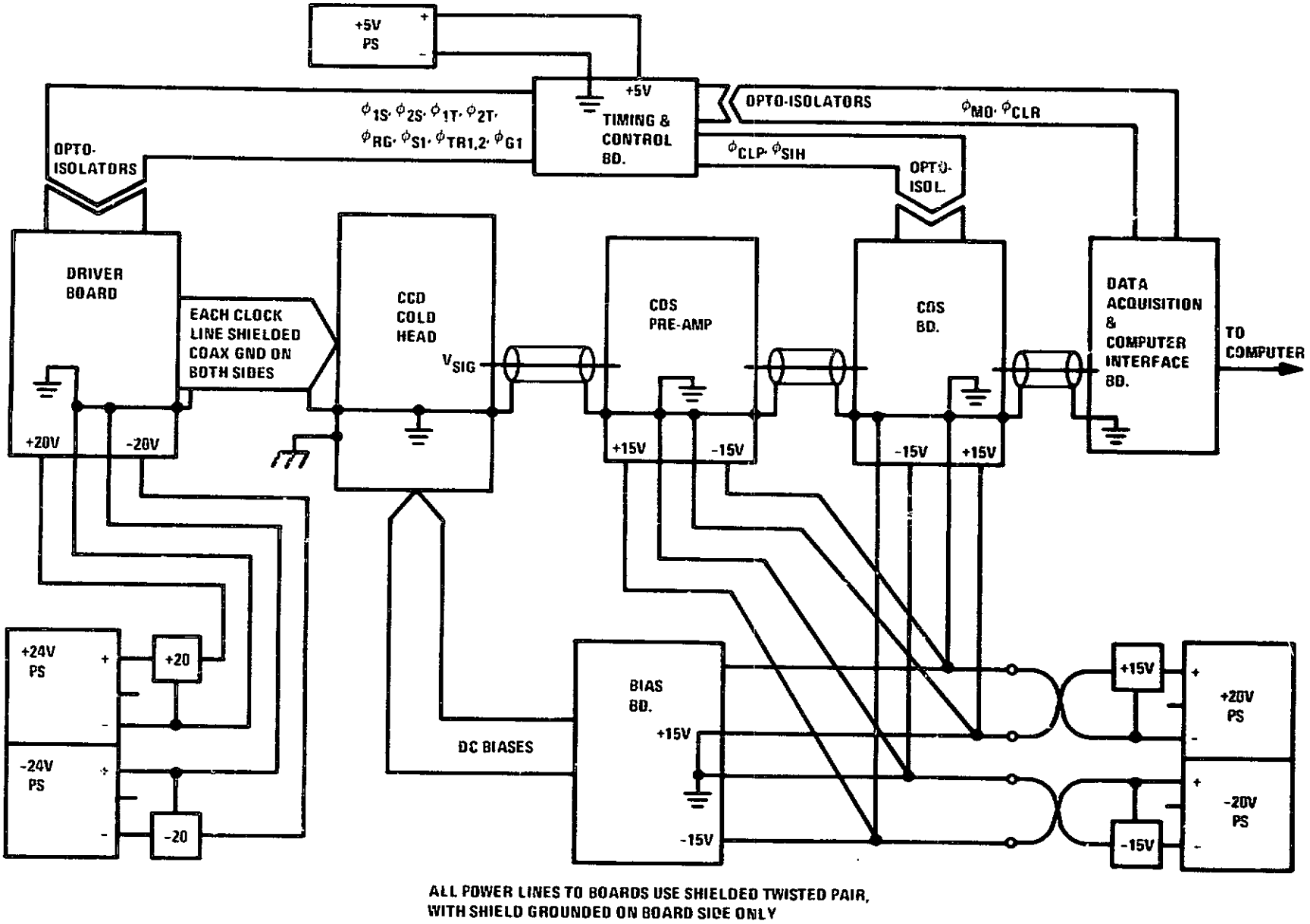


Fig. 6-1. Test electronics block diagram.

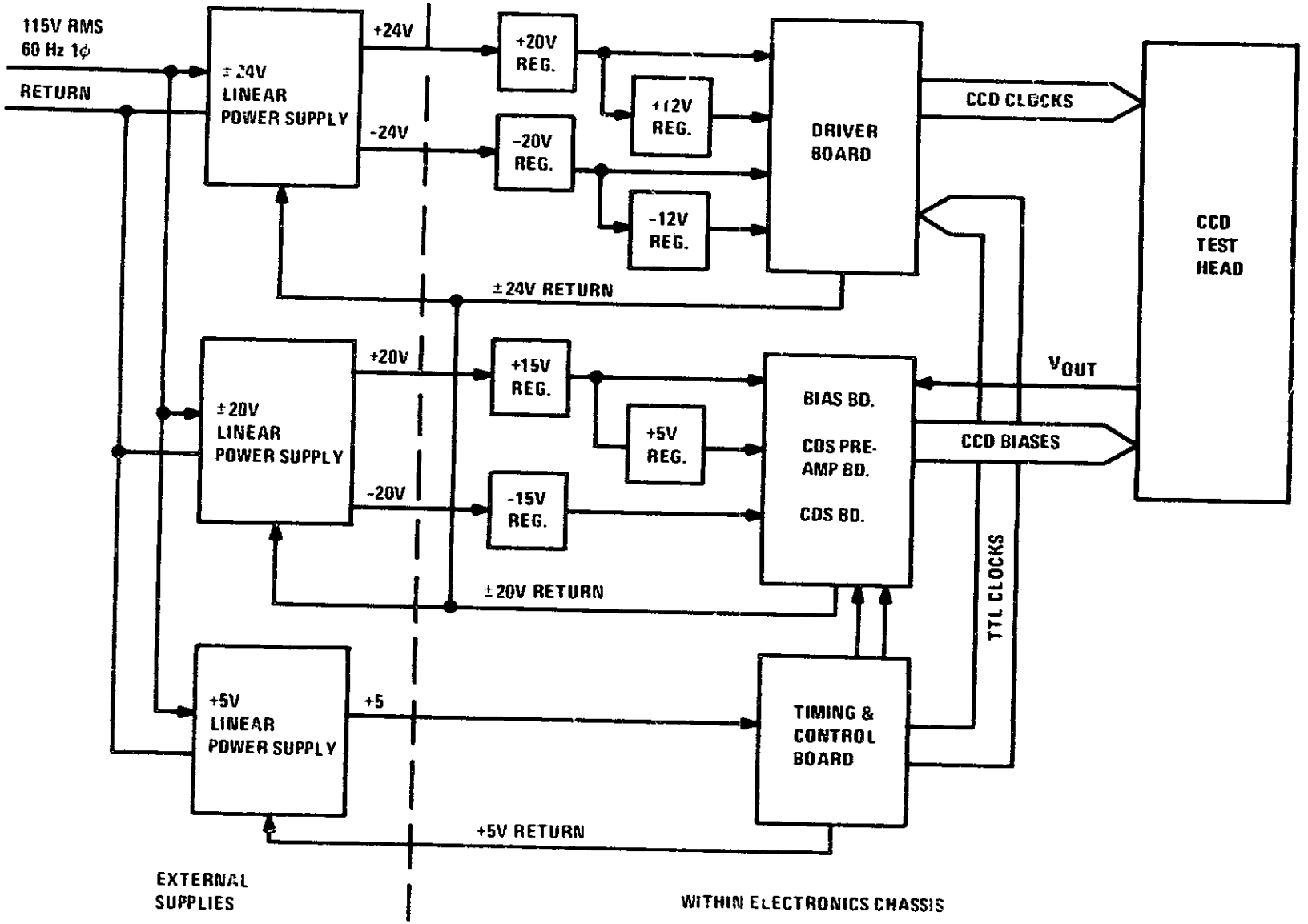


Fig. 6-2. Power conditioning.

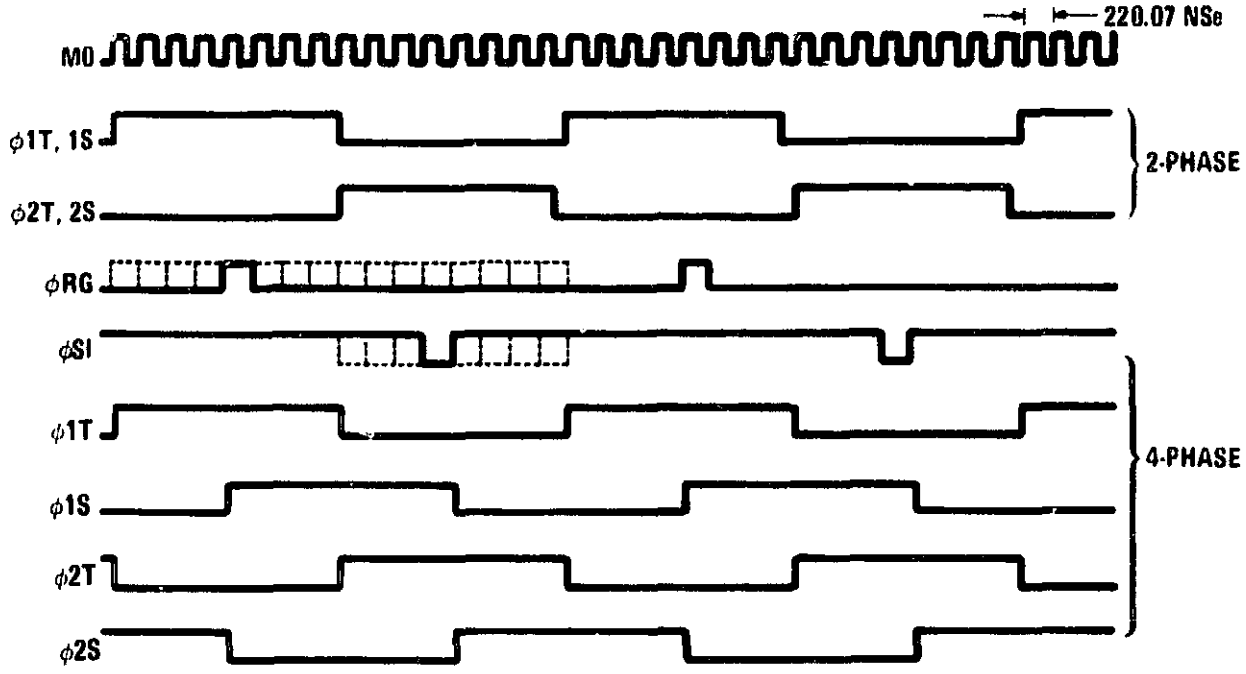


Fig. 6-3. CCD clocking scheme.

An option built into the CCD transfer clocking scheme is the choice of 2-phase or 4-phase operation. The relationships of ϕ_{1T}, ϕ_{2T}, ϕ_{1S}, and ϕ_{2S} for 2- and 4-phase clocking are shown in Fig. 6-3. These two approaches will be evaluated in an attempt to find the technique which optimizes CCD performance.

When operating the CCD in the 2-phase mode, the adjacent clocks (charge sending and receiving well, respectively) ϕ_{1T} and ϕ_{1S}, ϕ_{2T} and ϕ_{2S} will have increased edge overlap. In normal 2-phase complementary clocking the adjacent clocks overlap at the 50% point as shown in Fig. 6-4A. Published literature indicates that one method to improve transfer efficiency is to create the receiving well before the sending well has collapsed. This means that our overlap point changes from 50% to 75% as shown in Fig. 6-4B. The 75% complementary overlap clocking scheme will be implemented on the TA11567 SWIR tester and then evaluated. It is theorized that this further effect will enhance device operation.

Three different methods were proposed in the design of the timing and control circuitry. The first and most direct approach was to use standard TTL gates and switches and have limited system flexibility. Along with limited flexibility, the chip count of at least 30 made this approach undesirable. The second method using an EPROM to store waveforms and a RAM to read them out decreases the overall number of chips by 30% and gives the required flexibility. However, EPROM programming of waveforms is difficult. The third

a. Standard overlap (50%).

b. Shifted overlap (75%).

Fig. 6-4. Complementary clocking for 2-phase operation.

method, the one chosen, will use two field programmable logic arrays (FPLAs). This method was selected because it gave the required flexibility and reduced chip count, as in the EPROM method, but it also lends itself to relatively easy firmware programming (because it is a matrix of AND-OR gates and not addressed memory locations). The FPLA approach has been previously used in other Government contracted IRCCD systems. The main disadvantage of this method is that the FPLAs introduce small variable propagation delays due to the randomness of the blown AND-OR gates. This problem is alleviated by placing flip-flops at the outputs of the FPLA and reclocking these signals on the negative edge of the master oscillator (MO). This scheme introduces a small synchronous delay (100 ns) relative to the data acquisition circuits and is not seen as a problem. The two incoming signals are the master oscillator at a nominal rate of 4.5 MHz and the clear line. These signals originate in the data acquisition system and synchronize the CCD timing. A preliminary schematic is shown in Fig. 6-5.

6.3 DRIVER BOARD

This board will take the TTL level waveforms ϕ_{1T}, ϕ_{2T}, ϕ_{1S}, ϕ_{2S}, ϕ_{TR1}, ϕ_{TR2}, ϕ_{TR3}, ϕ_{RG}, ϕ_{S1}, and ϕ_{WD} and convert them to MOS levels which have pulse amplitude controls from 0 to 12 V and offsets from -15 V to +5 V.

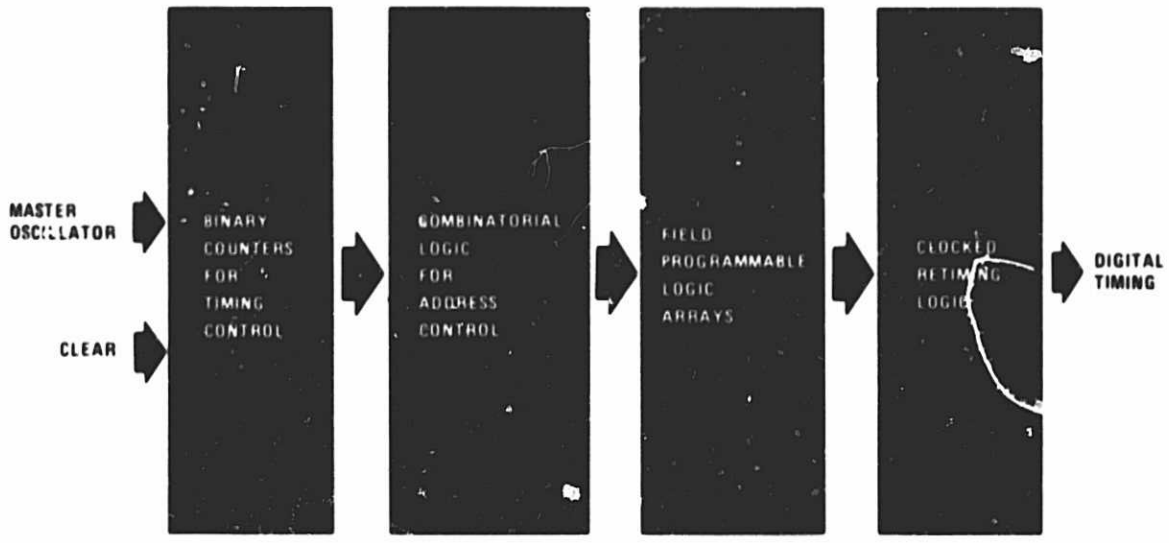


Fig. 6-5. Timing and control functional schematic.

Since it is ultimately required to drive five dual-band line arrays, each clock phase will drive an equivalent of 10 register gate loads. The gate capacitance for a typical clock phase is:

- Poly-to-substrate – 0.23 pF/mil^2
- Poly-to-poly – 0.083 pF/mil^2

Using the upper limit CCD register dimensions, the gate capacitance is calculated as

$$TC_{g \text{ to } s} = (106\ \mu m + 24\ \mu m)(10\ \mu m) \times 512 \text{ stages} \times \frac{0.23\ pF}{mil^2} \times \frac{1\ mil^2}{625\ \mu m^2} = 245\ pF$$

$$TC_{s \text{ to } s} = 2(106\ \mu m * 24\ \mu m)(3\ \mu m) \times 512 \text{ stages} \times \frac{0.083\ pF}{mil^2} \times \frac{1\ mil^2}{625\ \mu m^2} = 13.25\ pF$$

The total maximum capacitance load on an MOS driver is thus

T_{cd} = 2 bands x 5 chips x (245 pF + 13.25 pF)/chip-band = 2500 pF.

The total AC power dissipation is $= CV^2F$

$= (2500\ pF)\ (400\ V^2)\ (300\ kHz)$

$= 300\ mW$

The clock driver chosen is the National DS0026J. To evaluate its drive capability with a 2500-pF load and 300-mW power dissipation a test circuit was built. Three different capacitance loads were used: C = 0 pF, 1800 pF, 2800 pF. As seen in the photographs in Fig. 6-6, the edge speeds for C_L = 0 pF, 1800 pF, 2800 pF are 20 ns, 60 ns, 110 ns, respectively. For the 2500-pF requirement the edge speeds will not adversely effect CCD performance. In fact, the CCD clock phases generally have between 50- to 200-ns rise/fall times. The power dissipation for DUAL packaged drivers is approximately 700 mW and will probably need heat sinking. The total driver board dissipation will be about 3 W.

6.4 BIAS BOARD

The bias board will supply the DC biases for the output amplifier and DC biases for clock phase offsets. It is proposed that certain biases be current buffered in a further effort to reduce common-mode noise pickup. A typical configuration using the LH0002 current buffer is shown in Fig. 6-7.

6.5 CORRELATED DOUBLE SAMPLER

There are two primary reasons to use a correlated double sampler (CDS). The first is that the CDS technique reduces 1/f and low-frequency noise from the on-chip amplifier. The second is that it eliminates "reset" or "KTC" noise from the on-chip resettable floating diffusion. The CDS systems for the contract are being developed by Ball Aerospace.

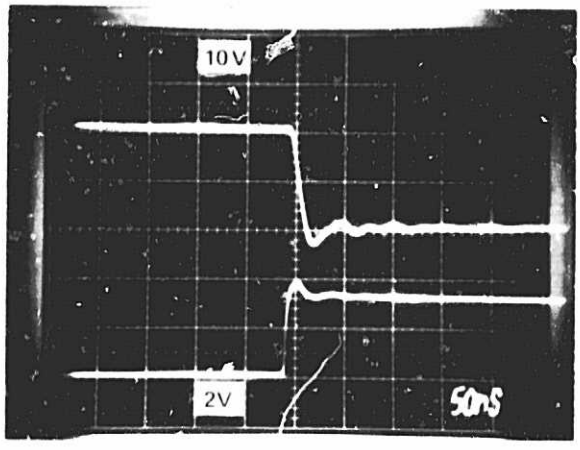
6.5.1 Preamplifier Design

The preamplifier has a low-noise differential FET pair for the input amplifier. The gain of the input cascode stage is about twenty. At this gain the CDS system noise is determined primarily by the input FET pair. An operational amplifier provides a large open-loop gain. The output is buffered by a unity gain power buffer. This buffer allows the preamplifier to drive low-impedance loads.

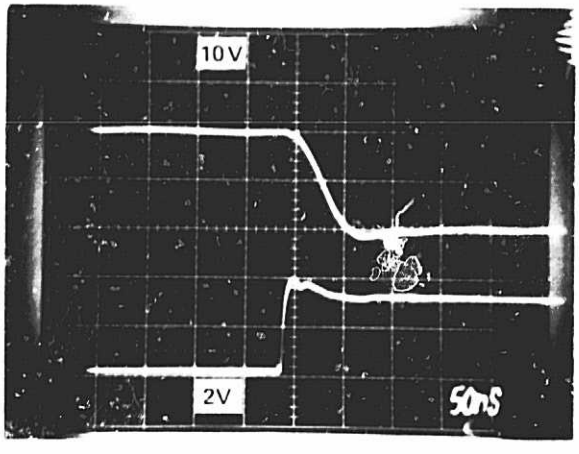
The input signal is attenuated by a step attenuator to allow control of the signal amplitude. A step attenuator is used because the input amplifier becomes unstable at low gains. The preamplifier gain is adjustable from zero (a calibrate position) to twenty in the following sequence: one, two, five, ten, and twenty. Figure 6-8 shows the preamplifier schematic.

The preamplifier has the following characteristics:

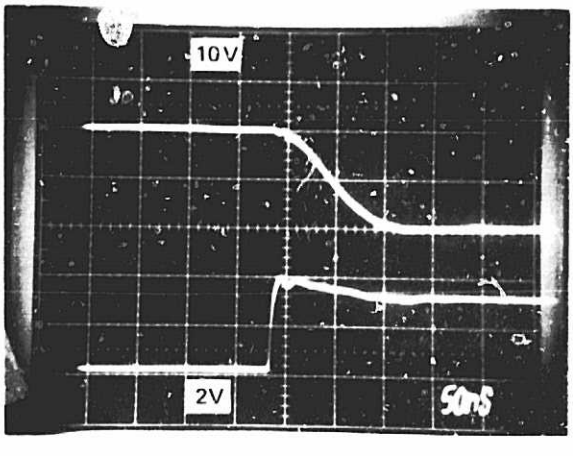
1. Gain: 20 (maximum).
2. Input noise: less than 10 μV rms (input referred).
3. Bandwidth: 700 kHz at the 3-dB point.
4. Power: plus and minus 15 V.



a. C_L = 0 pF
20 ns



b. C_L = 1800 pF
60 ns



c. C_L = 2800 pF
110 ns

Fig. 6-6. Edge response for different capacitive loads.

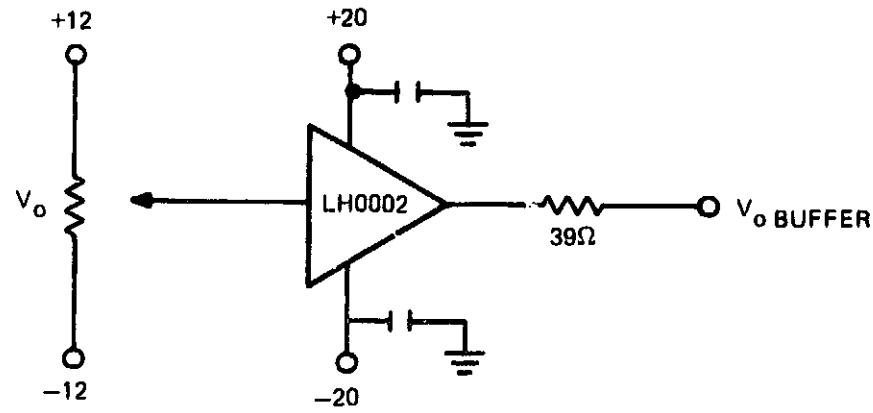


Fig. 6-7. Typical bias configuration for current buffer.

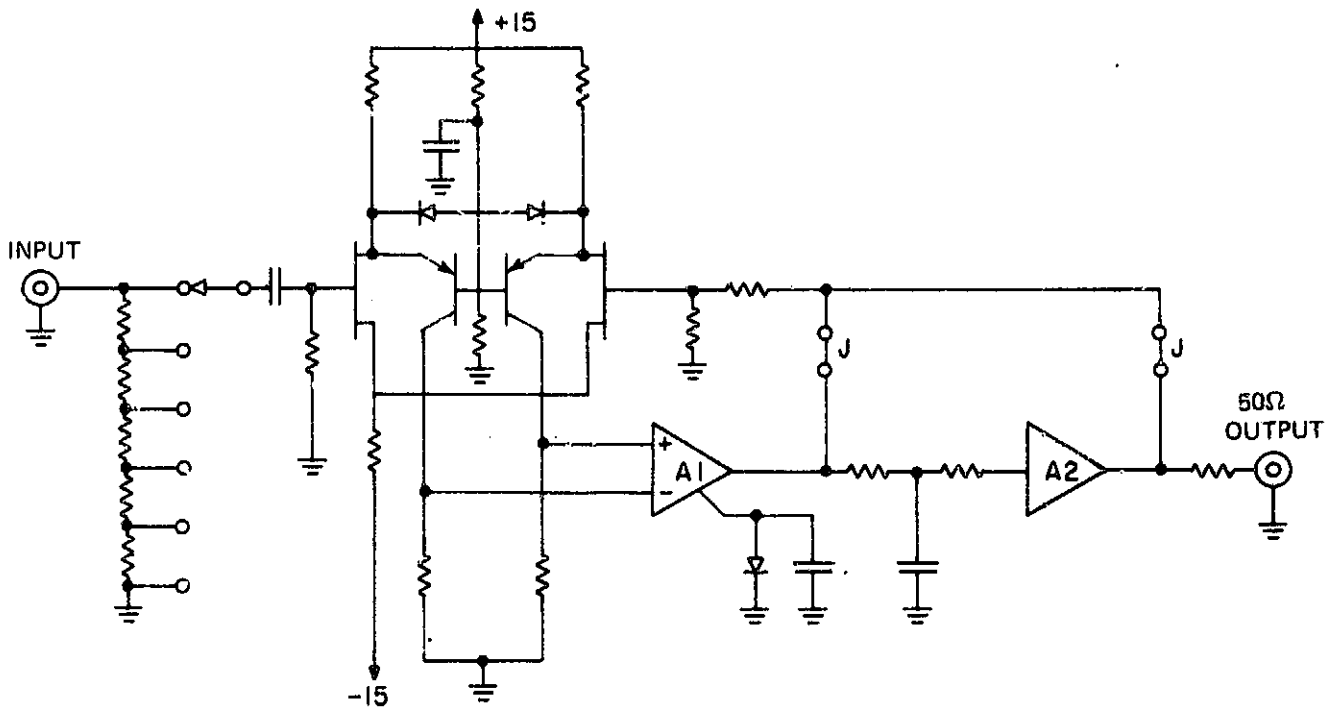


Fig. 6-8. Preamplifier schematic.

6.5.2 CDS Design

The input stage of the CDS (shown in Fig. 6-9) consists of A1 and its associated components, including the input attenuator. It is similar to the preamplifier except that no transistor buffering is required since the noise of this stage is quite small compared to the noise at the input of the preamplifier. The maximum gain of this stage is ten. The gain steps are: one, two, five, and ten. A bandwidth limiting capacitor has been placed in the feedback loop to limit the high-frequency bandwidth of the system.

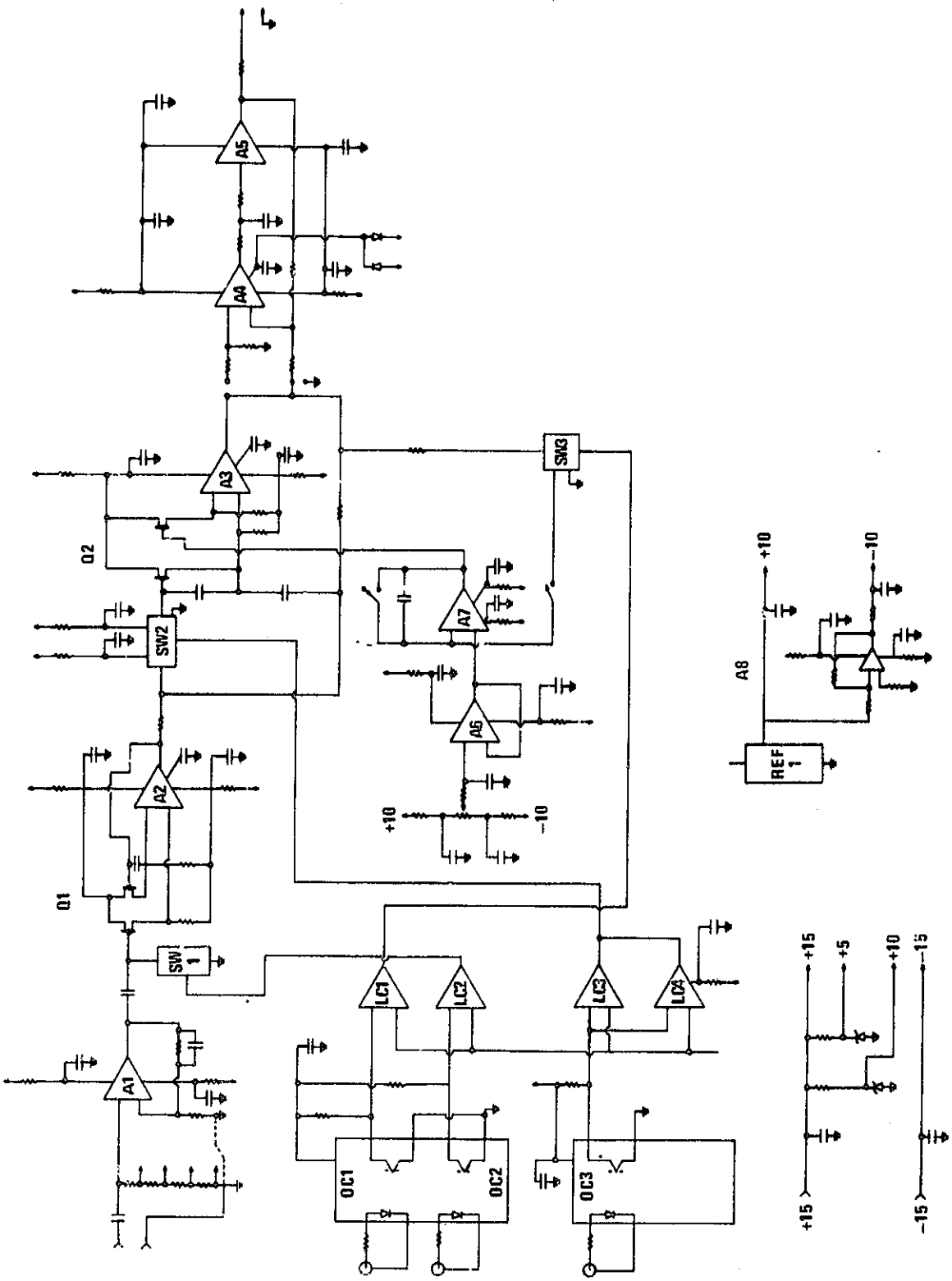


Fig. 6-9. Correlated double sampler.

The second stage of the CDS consists of SW1, Q1, and A2. SW1 provides DC restoration when the clamp signal is present. Q1 reduces the effect of the input leakage current of A2. A2 increases the open-loop gain of the second stage and lowers the drive impedance to the third stage. This stage has a gain of one.

The third stage consists of a buffered operational amplifier and an analog switch. This stage is the "hold" of the "sample-and-hold." The analog switch is used to disconnect the integrating capacitor in the "hold" mode, and Q2 provides the buffering to reduce the input leakage of A3.

The second and third stages together are a "clamped sample-and-hold." The second stage clamps input of the third stage to zero during the clamp pulse, and the third stage samples the voltage during the next sample pulse and holds the change in voltage until the next sample pulse.

The fourth stage consists of A4 and A5. This stage is used to buffer the signal from the output of A3 and can also be used to invert this signal. A5 increases the drive capability of the CDS. This allows the use of positive or negative signals to drive the external analog-to-digital converter or video processor.

A baseline stabilization stage consisting of SW3, A6, and A7 is provided to correct for drift. "Over-clocked pixels" are used to provide the reference level. A6 provides a variable DC reference to A7. SW3 is used to gate the over-clocked pixels to the integrator A7. A baseline restore signal must be provided when over-clocked pixels occur to use this feature.

The reference voltages for the integrator are derived from a precision voltage source, REF1, and an inverting amplifier, A8. These voltages are plus and minus 10 V nominal and are quite stable.

The control signals are fed through optical couplers OC1, OC2, and OC3 to a TTL to a CMOS level converter, LC1, LC2, LC3, and LC4. The output of these level converters are fed to the analog switches used to control the signal processing of the CDS. This was done to eliminate potential ground loops on the control signal lines.

Logic supply voltages are provided by separate zener diode supplies. This was done to ensure that there could be no interaction between the logic and the analog portions of the CDS.

6.5.3 Correlated Double Sampler Performance

Acceptance testing of the bread board Ball Aerospace correlated double sample (CDS) was conducted at Ball Aerospace Division (BASD). The circuitry was evaluated for noise reduction performance utilizing the high-density IRCCD test chip (TA11395). The noise level at the output of the CDS was measured first with the two-stage surface-channel floating diffusion amplifier connected and then the single-stage buried-channel floating diffusion amplifier connected.

Both measurements were done at room temperature with the floating diffusion reset FET clocked at a rate corresponding to a 1.8-ms integration time. The measurements were made utilizing a multichannel analyzer. The measured performance is detailed in Table 6-1.

TABLE 6-1. MEASURED PERFORMANCE

Amplifier	Without CDS*	With CDS
Surface Channel FD Amplifier	320 $\bar{e}$	110 $\bar{e}$
Buried Channel FD Amplifier	128 $\bar{e}$	35 $\bar{e}$

Note: Conversion factor 1.15 μV/e

*Measured at Advanced Technology Laboratories

As indicated, the CDS reduced the surface-channel floating diffusion amplifier noise from 320 rms electrons down to 110 rms electrons. The CDS reduced the buried-channel amplifier KTC and 1/f noise to an impressive level of 35 electrons rms. This performance indicates that (1) Ball has provided a high-performance CDS signal processor; and (2) the choice of the buried-channel amplifier is indeed justified. One further observation should be made. The SWIR proposal estimate for the CDS processed floating diffusion amplifier noise was 100 electrons rms; thus, we have exceeded the design goal.

The test conditions are detailed in Table 6-2. The test configuration is shown in Fig. 6-10 and Fig. 6-11. The details of the initial test results are shown in Table 6-3 along with a summary of these measurements.

TABLE 6-2. TEST CONDITIONS FOR TA11395 (G54) WITH CDS PROCESSOR

330-kilopixels/s readout rate
V_{D1}, V_{D2}, V_{DR}: 16 V
V_{GG}, V_{SS}: Ground
V_{sub}: -0.10 V
ϕ_{DC}: -6 V
ϕ_{RG}: -0.5 to +15 V, 200-ns width

Note: The output serial register was unclocked.

TABLE 6-3. INITIAL TEST RESULTS

Condition	Total gain	Preamplifier gain	CDS gain	Input reference* Total noise	CCD noise	(Referred to CCD) Preamplifier noise
1. Preamplifier input open	40	20	2	25 e rms	–	25
2. Preamplifier input shorted	40	20	2	21	–	21
3. Preamplifier input shorted (10KΩ)	40	20	2	23	–	23
4. SOX output (buried-channel)	40	10	4	45	(35	(28
5. SOX output (buried-channel)	40	20	2	38	35)	14)
6. Preamplifier input shorted (10K)	40	10	4	34	–	34
7. SOX output (buried-channel)	20	5	4	85	35	(77)
8. SOA output (surface-channel)	40	10	4	116	(111)	34
9. SOA output (surface-channel)	50	5	10	126	(106)	(68)
10. SOA output (surface-channel)	20	5	4	129	(110)	(68)

*Assuming 1.15 μV/e^- on-chip sensitivity

Measurement Summary

Lines 4 and 5: Entries in parentheses were derived from the following:

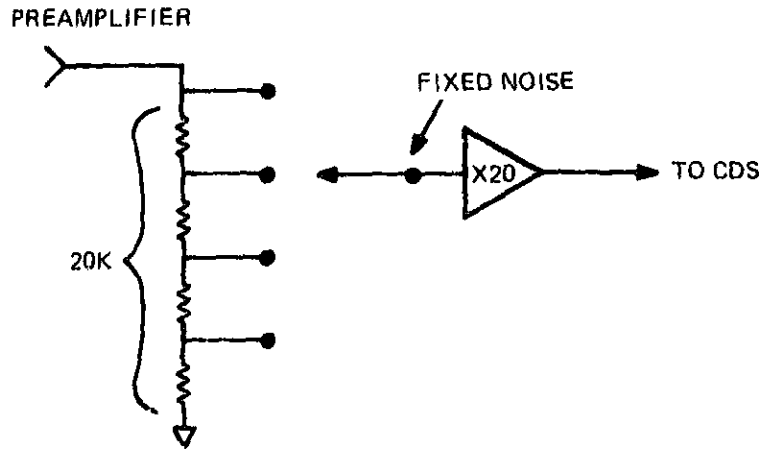
$$45 = \sqrt{P^2 + C^2}$$
$$38 = \sqrt{\left(\frac{P}{2}\right)^2 + C^2} \longrightarrow \begin{matrix} C = 35 \\ P = 28 \end{matrix}$$

where P = input referred preamplifer noise with preamplifier gain = 10
C = chip noise

Line 6: Measured value of 34 is ∿ 28 derived above. (This does not seem to be inconsistent with the derived value of lines 4 and 5.)

Line 7: With a preamplifier gain of 5, the preamplifier noise (input referred) should be up 4X compared to the preamplifier gain of 20. Assuming 35 as chip noise, 77 is derived for preamplifier noise. This is ∿ 2X 34, but more than 4 x 14 = 56.

Lines 8 to 10: The lines assume 34 as the input referred preamplifier noise, and give consistent results for the chip noise (SOX).



Preamplifier noise, referred to preamplifier input, depends on preamplifier gain setting (attenuator setting).

Fig. 6-10. Preamplifier gain adjustment.

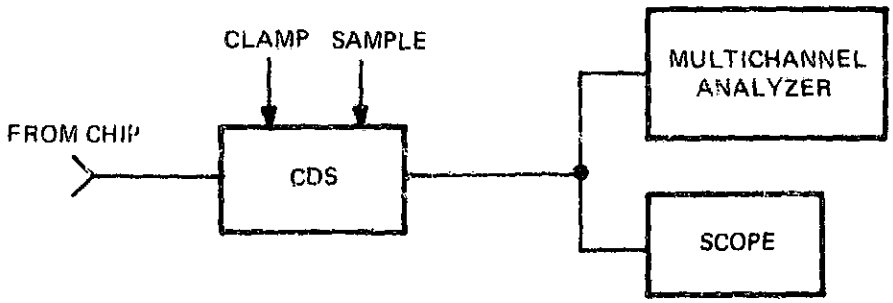


Fig. 6-11. Test configuration.

6.6 CCD OPERATING POTENTIALS

Tables 6-4 and 6-5 show the voltage range requirements for the 512-stage, dual-band short wave infrared sensor. Ten AC clocks with amplitude and offset control are required for proper operation. ϕ_{1S}, ϕ_{1T}, ϕ_{2S}, and ϕ_{2T} are the first and second poly-silicon storage and transfer gates responsible for clocking charge serially through the CCD. ϕ_{RG} resets the output floating diffusion. Three gates – ϕ_{TR1}, ϕ_{TR2}, and ϕ_{TR3} – are located between the CCD and the detector elements. These are used to "dump" the infrared signature into the CCD registers. Through proper biasing of these three gates, charge skimming or pulsed vidicon operation are possible. ϕ_{S1} is a strobing clock used when injecting charge into the CCD register. ϕ_W is a periodic pulsed waveform with varying amplitude, offset, period, and duty cycle. It is injected through the input stage at G_1. Proper biasing of ϕ_{S1} and ϕ_{WD} is necessary to make transfer efficiency measurements as well as other tests.

The remaining biases of the CCD are DC. V_{G2} is an input stage bias. V_{DC1} and V_{DC2} are located before the floating diffusion and are used to ensure charge from the CCD is properly injected on to the output floating diffusion.

TABLE 6-4. DUAL-BAND SENSOR CLOCK BIAS RANGES

Clock	Offset Range (V)	Amplitudes (V)
ϕ_{1S}	V_{1SB} (0, -12)	V_{CLK} (0, 16)
ϕ_{1T}	V_{1TB} (0, -15)	V_{CLK} (0, 16)
ϕ_{2S}	V_{2SB} (0, -12)	V_{CLK} (0, 16)
ϕ_{2T}	V_{2TB} (0, -15)	V_{CLK} (0, 16)
ϕ_{RG}	V_{RGB} (-12, 6)	V_{RGA} (0, 12)
ϕ_{TR1}	V_{TRB} (-12, 6)	V_{TR1A} (0, 20)
ϕ_{TR2}	V_{TRB} (-12, 6)	V_{TR2A} (0, 20)
ϕ_{TR3}	V_{TRB} (-12, 6)	V_{TR3A} (0, 20)
ϕ_{S1}	V_{S1B} (0, 16)	V_{S1A} (0, 16)
ϕ_{WD}(G1)	V_{WB} (-4, 4)	V_{WA} (0, 5)

TABLE 6-5. DUAL-BAND SENSOR DC BIAS VOLTAGES

Bias	Range
V_{G2}	(-10, 10)
V_{DC1}	(-12, 12)
V_{DC2}	(-12, 12)
V_{FS}	(-12,0)
V_{ED}	(SUB, +15)
V_{RDC}	(+12, 20)
V_{DR}	(+12, 20)
V_{DD}	(+12, 20)
SUB	(-6, 0)

V_{FS}, the field shield voltage, which biases the regions between the individual detector elements, is used to minimize detector crosstalk. V_{ED}, edge drain bias, minimizes the dark current generated at the silicon butt edges due to device sawing. V_{RDC}, a gate located between the reset channel and V_{DR} (the reset drain), is biased so that the output floating diffusion is properly reset. V_{DD} is the output amplifier drain voltage, SUB; the substrate potential is usually biased around ground.

6.7 BENCH TEST AND CALIBRATION OPTICAL EQUIPMENT

The test configuration to be used in measuring the transfer characteristics, response uniformity, signal-to-noise, and dynamic range is shown in Fig. 6-12. In this arrangement three different bandpass filters – 1.2 to 1.3 μm, 1.55 to 1.75 μm, and 1.55 to 1.75 μm – are used to define the spectral bands of interest; the irradiance at the detector array is varied by the aperture wheel and neutral density filters. Measurement of detector irradiance requires placing the detector head of the calibrated radiometer at the same distance from the source as the detector array. In the actual substitution, the source rather than the detector array will be moved since the detector array will be contained in the cold head of the cryogenic cooler.

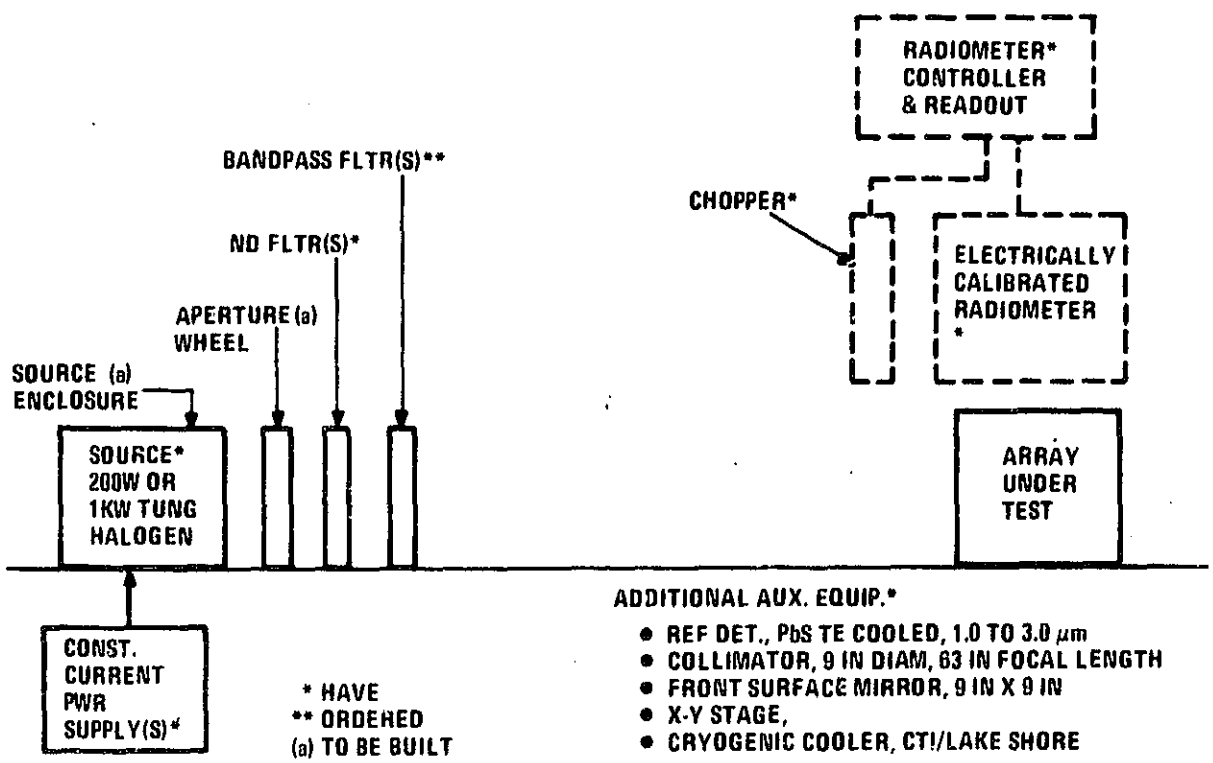


Fig. 6-12. Basic test configuration for measurement of transfer characteristics, response uniformity, signal-to-noise, and dynamic range.

With the exception of the three bandpass filters, all of the equipment (purchased as part of the RCA Capital Expenditure Budget) has been received. The three custom-made bandpass filters were ordered on 1 December 1982 and their completion is expected shortly. The enclosure which contains the tungsten-quartz halogen lamp has been designed and will be built by RCA.

The irradiance in each of the three spectral bands resulting from the 200-W quartz halogen source is shown in Table 6-6A at both 50 cm and 150 cm from the source. At the 150 cm, the irradiance exceeds the working level irradiance (WLI) of each of the bands and, accordingly, neutral density filters and/or adjustment of the distance would be required to attain WLI. The 1000-W source is intended, principally, to provide sufficient irradiance at the detector array to determine the saturation irradiance while maintaining a source-to-array separation large enough to assure uniform illumination across the array. As may be seen in Table 6-6B, even at the relatively large separation of 300 cm, the detector irradiance in each of the bands exceeds two times the minimum full-scale irradiance (MFSI) by a comfortable margin. In fact, at 150 cm the 200-W source may also be used for measurements at and around MFSI.

TABLE 6-6. IRRADIANCE AT SELECTED DISTANCES FROM SOURCE IN EACH OF THE THREE SPECTRAL BANDS FOR 200-W AND 1000-W QUARTZ HALOGEN LAMPS

A. STANDARD OF SPECTRAL IRRAD. 200W QUARTZ HALOGEN
OPTRONIC LABS. MDL 220B (PWR SUPPLY MODEL 65)
CALIBRATED AT 50 cm & 6.50 Adc

BAND (μm)	I @ 50 Cm (μW/Cm^2)	I @ 150 Cm (μW/Cm^2)	WLI (μW/Cm^2)
1.2-3.0	394	44	9.2
1.55-1.75	478	53	7.2
2.08-2.35	305	34	3.5

B. STANDARD OF SPECTRAL IRRAD. 1000W QUARTZ HALOGEN
OPTRONICS LABS MDL 200H (PWR SUPPLY MODEL 83 DS)
CALIBRATED AT 50 Cm & 8.00 Adc

BAND (μm)	I @ 50 Cm (mW/Cm^2)	I @ 300 Cm (μW/Cm^2)	2X MFSI
1.2-1.3	2.09	58	28
1.55-1.75	2.50	69	22.4
2.08-2.35	1.59	44	12.6

The characteristics of the calibrated pyroelectric radiometer, the neutral density and spectral bandpass filters, and of the source enclosure, all of which are to be used in the basic test configuration of Fig. 6-12 are summarized in Table 6-7. A listing of other in-house equipment planned for use in array testing and in the evaluation and image making phases of the program is given in Table 6-8.

6.7.1 Bench Test and Calibration Equipment Scene Simulator

To produce imagery from a 512-stage line array it is necessary to scan an image using a mirror (rotational scan) as shown in Fig. 6-13a or move the image across the face of the array (translational scan) as shown in Fig. 6-13b. Rotational scans can cause slight aberrations because the effective distance (image to lens) changes as a function of mirror angle. Translation scanning has the disadvantage of limiting one's choice of targets. However, this method is similar to a satellite-type scan and may be more appropriate to analyze. After choosing between rotational scan and translational scan, it is possible to implement either in a digital mode (using a stepper motor) or an analog mode. Use of a stepper motor would produce imagery that could require horizontal filtering, whereas the analog scan would tend to smooth the image in the direction of the scan.

Use of analog scanning in the SWIR bench test and calibration equipment laboratory would introduce a difficulty. The computer which processes these data accepts a maximum of 32K pixels and then performs some minor "housekeeping" functions before accepting another 32K pixel burst. Therefore, only 64 (64x512 = 32K) continuous lines can be accepted per scan. To produce a 512-x-512 image would require eight scans. Synchronizing electronics would have to be built so that the 64th line of the ith pass would be adjacent to the first line of the (ith + 1) pass.

In specifying stepper stages for translational and rotational scans it is first necessary to calculate the minimum resolution. For the rotational scan, the minimum resolution, R_r, is:

$$R_r = 0.11°/\text{step}$$

The minimum translational resolution, T_r, is:

$$T_r = 0.5\ \text{mm/step}$$

Another important scanner specification is the single-step settling time for stepper stages. Nominal settling times are 2.5 ms. Under this restriction the array would integrate (1.8 ms) and dump three lines. The first two lines would be ignored since they occur during the settling time of the step; the third valid dump would be read to the computer.

TABLE 6-7. CHARACTERISTICS OF RADIOMETER, FILTERS, AND SOURCE ENCLOSURE

- **ELECTRICALLY CALIBRATED PYROELECTRIC RADIOMETER**
  - LASER PRECISION MDL RS-5900 OPTNS RJI-700 (BCD-S/P), & RSV (EVACUABLE PROBE)
  - NBS TRACEABLE CALIBRATION
  - MIN. IRRAD. 20 nW/Cm^2, MAX IRRAD. 200 mW/Cm^2
  - PROBE LITHIUM TANTILATE PYRO, 0.5 Cm^2, SUPRASIL WINDOW
  - CHOPPER, FIXED SPd., 15 Hz
  - READOUT, TUNED LOCK-IN VM NULL DET & MICRO-PROC. MEAS. & CNTRL WITH BCD SER. TO PARL. CONVERTER
- **NEUTRAL DENSITY FILTERS**
  - SET OF 7, 0.1, 0.2, 0.3, 0.4, 0.5, 1.0 & 2.0 (2 IN X 2 IN)
  - TRANS. MEASURED FRM. 0.6 μm TO 2.60 μm

λ (μm)	D = 0.1 (0.794)	D = 0.5 (0.316)	D = 1.0 (0.10)
1.25	.850	.360	.108
1.65	.870	.380	.098
2.20	.863	.386	.087

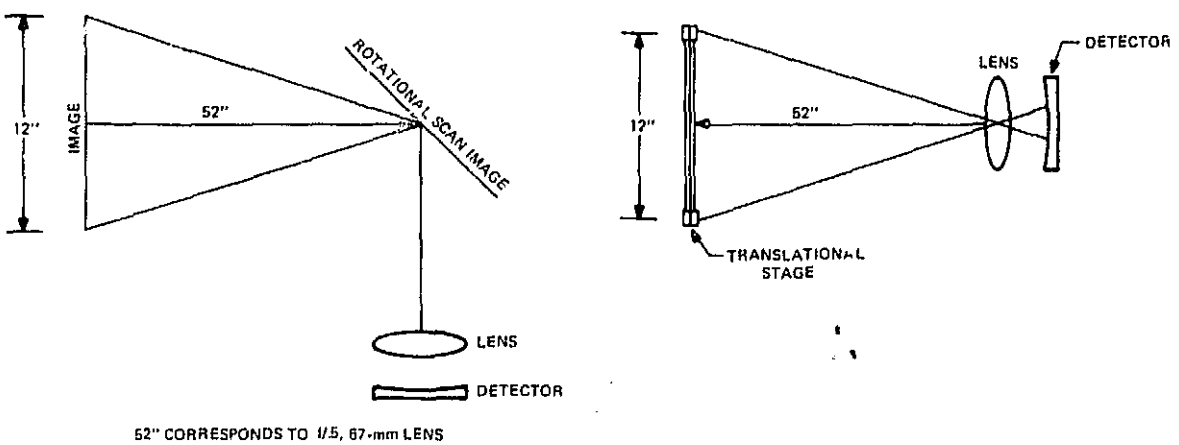
- **BANDPASS FILTERS (ORDERED)**
  - 1/2 PWR. PTS. TO ±2%,
  - OUT OF BAND REJ. $<10^{-3}$,
  - SLOPES 6%
  - SIZE 2 IN X 2 IN

BAND (μm)	TRANS. (%)
1.20-1.30	50
1.55-1.75	60 TO 70
2.08-2.35	60 TO 70

- **SOURCE ENCLOSURE (TO BE BUILT)**
  - SIZE, APPROX 5x5x14 IN
  - MTL, BLK. ANODIZED AL. EXTRD. HT. SNK TYPE
  - APERTURE WHEEL OR INSERTS BUILT-IN
  - AIR COOLING WITH BUILT-IN BLOWER

TABLE 6-8. OTHER IN-HOUSE EQUIPMENT PLANNED FOR ARRAY TESTING AND EVALUATION

- MONOCHROMATOR (SPECTRAL RESPONSE TESTS)
  - SPEX MODEL 1700-II
    CZERNY-TURNER TYPE, 75 cm FOCAL LENGTH, F15.6
    GRATING 600 GROOVES/mm, COVERAGE 0.2 TO 2.8 μm
    MOTOR DRIVE (SERVOTEK FOR SPEX) MODEL 1513
- VARIABLE SPEED CHOPPER (TEMPORAL RESPONSE)
  - PRINCETON APPLIED RESEARCH – PAR 125
  - PHASE LOCKED VARIABLE SPEED CHOPPER DRIVER – PAR 222
- POINT SOURCE (CROSSTALK/BLOOMING, & DETECTOR PROFILING)
  - TROPEL MODEL 2001, WITH 45W QUARTZ HALOGEN LAMP
  - PIN HOLE APERTURE WHEEL (25, TO 800 μm, 7 STEPS)
  - 5 μm PROJECTED PIN HOLE DIAM., 50 μm APERTURE & 32 mm OBJECTIVE
  - 160 μm PROJECTED PIN HOLE DIAM, 800 μm APERTURE & 32 mm OBJECTIVE
- LENS (IMAGERY)
  - RESEARCH OPTICAL GROUP
  - 100 mm FOCAL LENGTH, F/1.50, 67 mm DIAMETER
  - TRANSMISSION 90%, 1.20 TO 4.80 μm
- MOTOR DRIVEN ROTATING DRUM (IMAGERY)
  - RCA ASSEMBLED
  - USED IN ESSWACS PRELIM CONCEPTS EXPERIMENTS



a. Rotational scan. b. Translational scan.

Fig. 6-13. Scanner geometrical requirements.

Shown in Table 6-9 is an initial compilation of instrumentation available to perform the various options. The most attractive approach to date is the purchase of the Daedel Inc., PC-209 stage driver. This driver has the ability to drive translational and rotational stages continuously or stepped.

Further investigations into the system specifications are necessary. A further study of the tradeoffs will be done before committing to an individual method of scene simulation. Some tradeoffs are cost, ease of implementation of chosen method, quality of imagery, and the importance in producing imagery similar to a satellite-borne system.

TABLE 6-9. AVAILABLE INSTRUMENTATION

	Translation		Rotation	
	Analog	Stepper	Analog	Stepper
Klinger		UT-100P 2.5 ms		UR-100P 0.01°/step 2.5 ms/step
Daedel	PC-209	PC-209 43021 Stage	PC-209	PC-209 Driver 20601 Stage
Ardel		TD-50M 1-μm resolution		RTM-175 0.1°/step
General Scanning	G300P		G300P Scanner AX-2000 Driver	

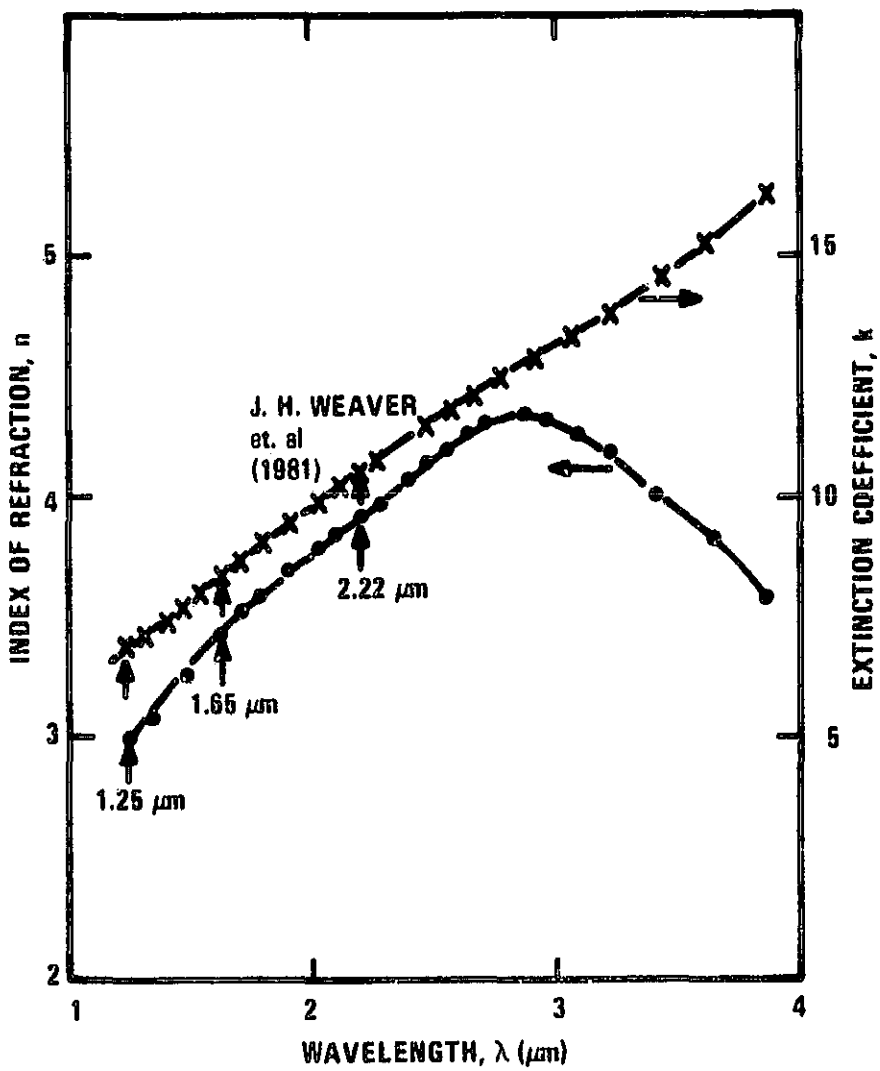
APPENDIX A

SUMMARY OF THE MAIN PROPERTIES OF Pt & Pd & Ir

	Ir	Pt	Pd
Atomic No.	77	78	46
Atomic Weight	192.22	195.09	106.4
Melting Point	2410°C	1772°C	1552°C
Boiling Point	4130°C	3827 ± 100°C	3140°C
Electronic Structure	$K_s 2$ $L_s 2$ $L_s 6$ $M^p 2$ $M^s 6$ $M^p 10$ $N^d 2$ $N^s 6$ $N^p 10$ $N^d 14$ $O^s 2$ $O^s 6$ $O^p 9$ O^d_f	$K_s 2$ $L_s 2$ $L_s 6$ $M^p 2$ $M^s 6$ $M^p 10$ $N^d 2$ $N^s 6$ $N^p 10$ $N^d 14$ $O^s 2$ $O^s 6$ $O^p 9$ O^d_f $P^f_s 1$	$K_s 2$ $L_s 2$ $L_s 6$ $M^p 2$ $M^s 6$ $M^p 10$ $N^d 2$ $N^s 6$ $N^p_d 10$
Density gm/cm^3	22.61	21.45	12.02
Etchant	Aqua-Regia & Conc. HCl+ $NaClO_3$ at 125-150°C	Aqua-Regia	Aqua-Regia & Conc. HNO_3, HCl+ Cl_2 at 125-150°C

APPENDIX B

Optical Properties of Pd-Crystal



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